

CHIPLINK P-Channel Enhancement Mode Power MOSFET

Description

The LX4805H combines advanced trench technology to provide excellent $R_{DS(ON)}$, it tailored to minimize conduction loss, and provide superior switching performance.

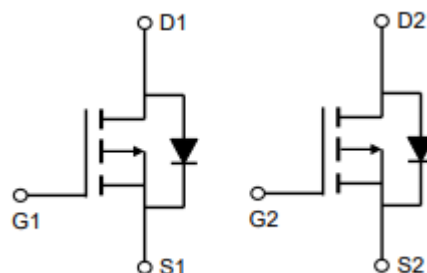
Features

- $V_{DS}=-30V$, $I_D=-9A$
 $R_{DS(ON)typ.}=14m\Omega@V_{GS}=-10V$
 $R_{DS(ON)typ.}=18.5m\Omega@V_{GS}=-4.5V$
- Fast switching
- High power and current handing capability
- Termination is Lead-free and RoHS Compliant

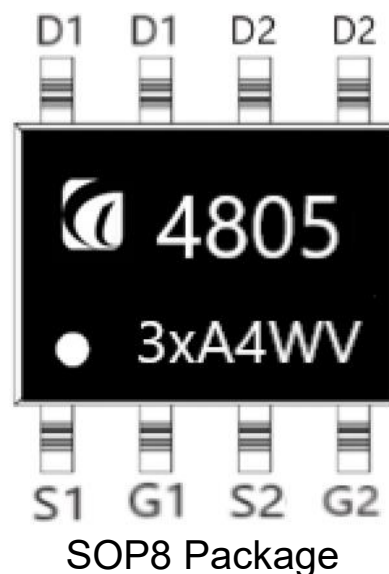


Applications

- PWM applications
- Load switch
- Power Management



Schematic Diagram



Maximum Ratings($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D(T_C=25^{\circ}C)$	-9	A
	$I_D(T_C=70^{\circ}C)$	-7	A
Pulsed Drain Current ^B	I_{DM}	-36	A
Maximum Power Dissipation ^A	P_D	2.0	W
Single pulse avalanche energy	E_{AS}	54	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction to Case	R_{QJC}	17	$^{\circ}C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate-Threshold Voltage	V _{th(GS)}	V _{DS} = V _{GS} , I _D =-250 uA	-1	-1.5	-2.0	V
Gate-body Leakage	IGSS	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	IDSS	V _{DS} =-30V, V _{GS} =0V			-1	uA
Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-9A		14	17	mΩ
		V _{GS} =-4.5V, I _D =-5A		18.5	21	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = -15V, V _{GS} =0V, F=1MHz		1770		pF
Output Capacitance	C _{oss}			231		
Reverse Transfer Capacitance	C _{rss}			215		
Switching Capacitance						
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15V, R _L =3Ω V _{GS} = -10V, R _{GEN} =3Ω		13		nS
Turn-on Rise Time	t _r			8.5		nS
Turn-off Delay Time	t _{d(off)}			26		nS
Turn-off Fall Time	t _f			12		nS
Total Gate Charge	Q _g	V _{DS} = -15V, I _D =-9A, V _{GS} =-10V		32		nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			10		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-9A			-1.2	V
Diode Forward Current	I _s				-9	A

Notes:

- The Power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using $\leq 10s$ junction-to ambient thermal resistance.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- The Static characteristics in Figures are obtained using $<300\mu s$ pulses, duty cycle 2% max.
- EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=-15V, V_{GS}=-10V, L=0.5Mh$.

Typical Electrical and Thermal Characteristics

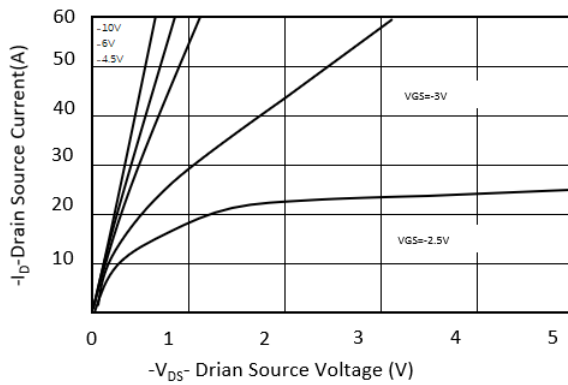


Figure 1: On-Region Characteristics

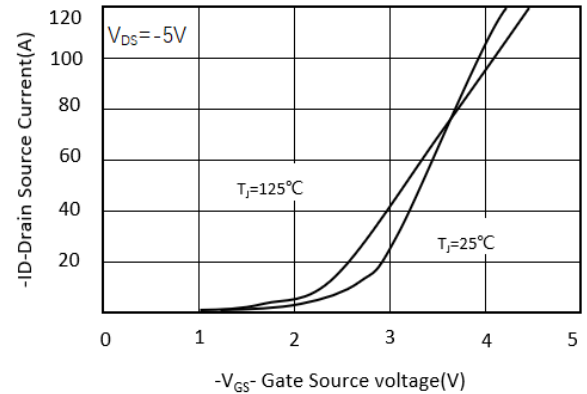


Figure 2: Transfer Characteristics

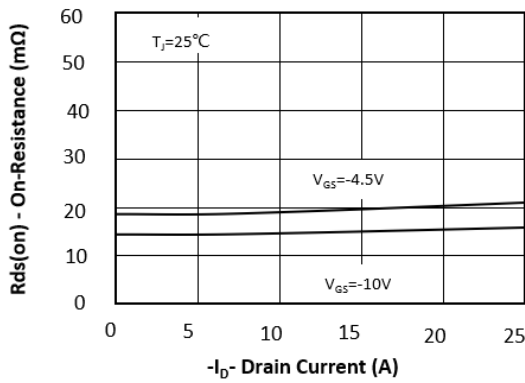


Figure 3. On-resistance vs. Drain Current

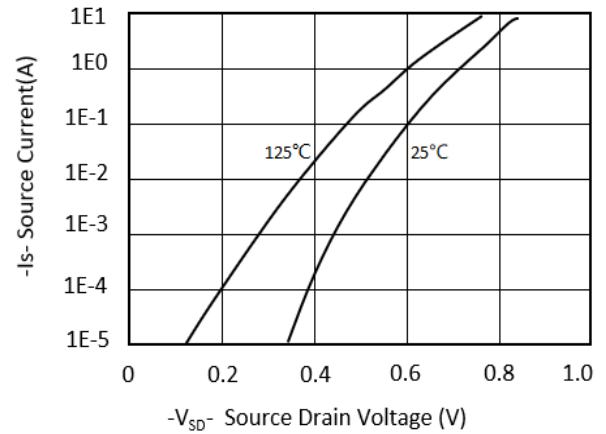


Figure 4. Body Diode Characteristics

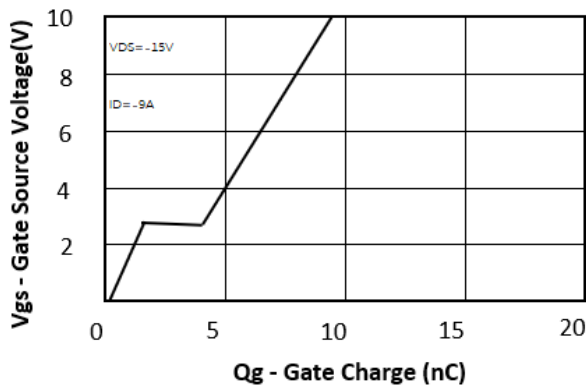


Figure 5. Gate Charge Characteristics

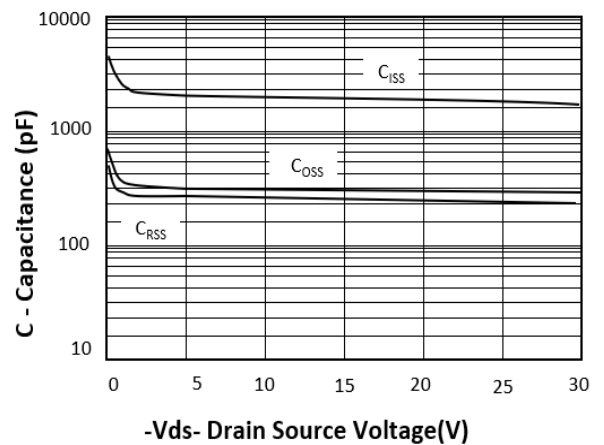


Figure 6. Capacitance Characteristics

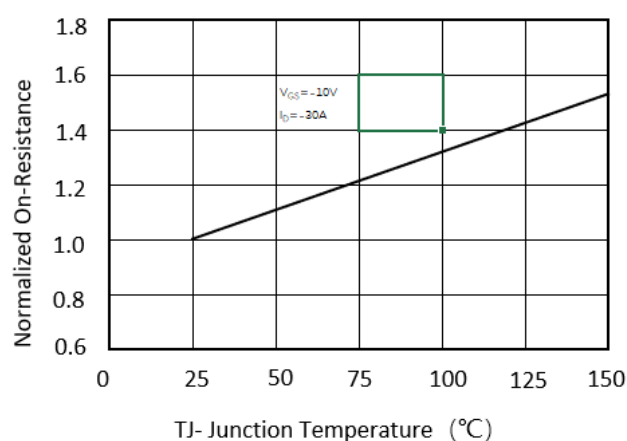


Figure 8: On-Resistance Vs. Junction Temperature

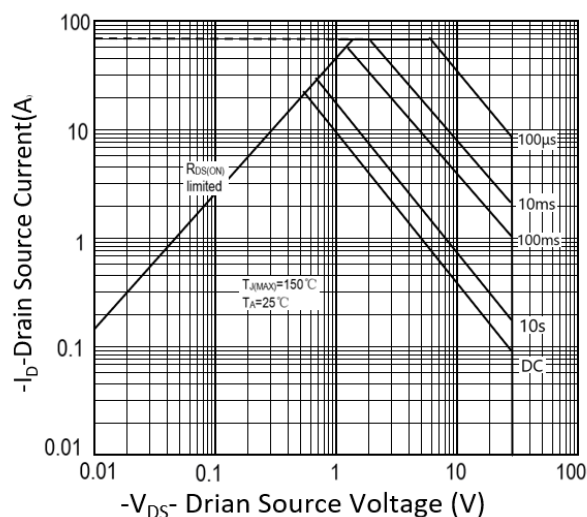
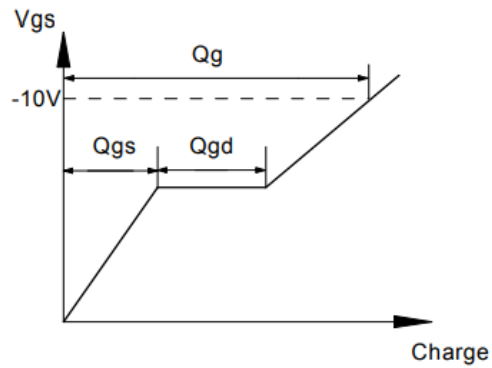
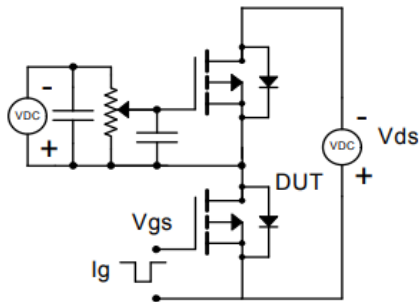


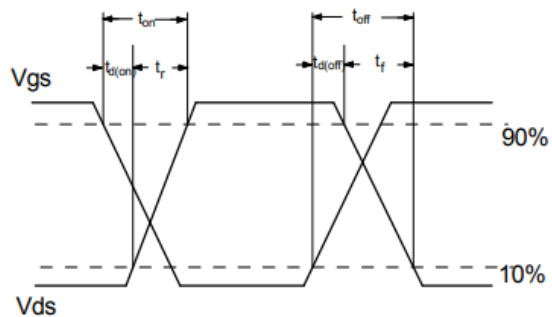
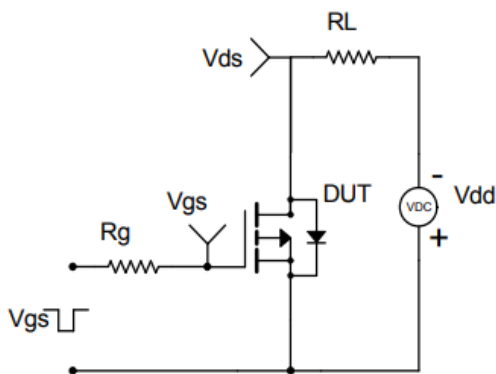
Figure 10. Safe Operation Area



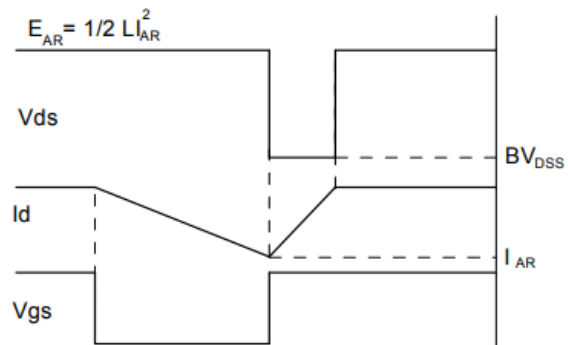
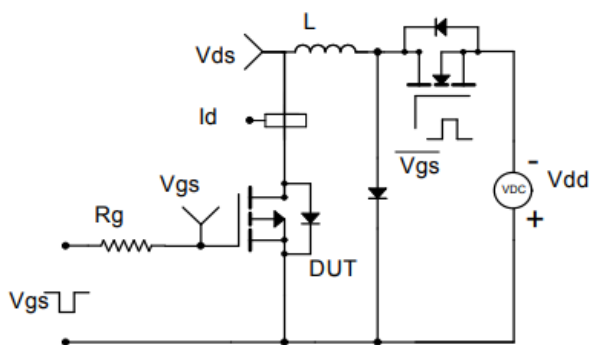
Gate Charge Test Circuit & Waveform



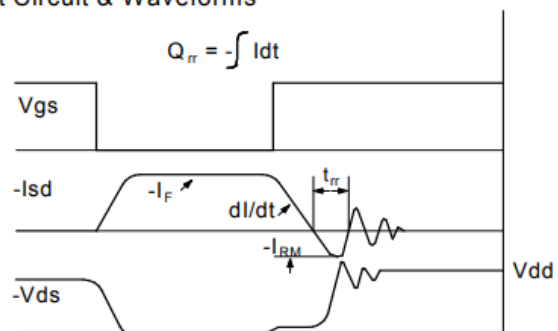
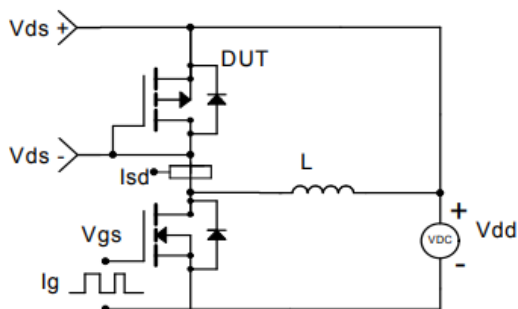
Resistive Switching Test Circuit & Waveforms



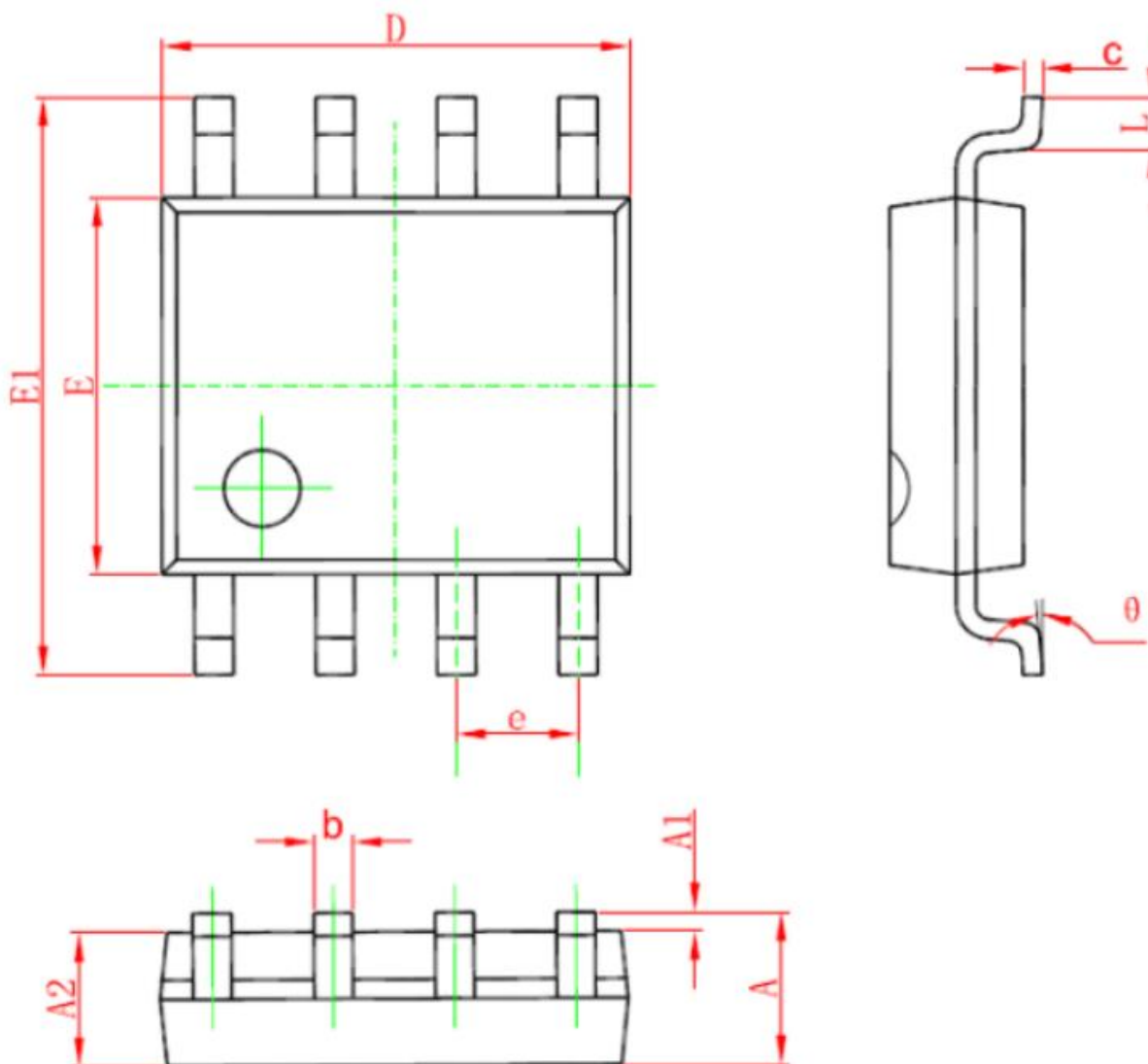
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOP8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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