

CHILINK N-Channel Enhancement Mode Power MOSFET

Description

The LX3080N1 combines advanced trench technology to provide excellent $R_{DS(ON)}$, it is tailored to minimize conduction loss, and provide superior switching performance. It can be used in a wide variety of applications.

Features

- $V_{DS} = 30V$, $I_D = 80A$
 $R_{DS(ON)typ.} = 3.7m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)typ.} = 5.3m\Omega @ V_{GS} = 4.5V$
- 100% Avalanche Tested
- Fast Switching
- Termination is Lead-free and RoHS Compliant

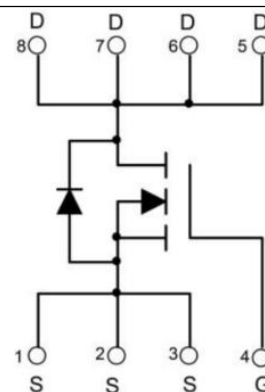


Applications

- PWM Applications
- Load Switch
- Power Management

Marking Description

Logo : ChipLink logo
 3080 : Part number code
 N1 : Packing code PDFN3333
 Y : Year code
 W : Week code
 V : Fab code
 XX : Lot code
 D : OSAT code



Schematic Diagram



PDFN3333 Package Marking Description

Maximum Ratings

($T_A = 25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D(T_C = 25^\circ C)$	80	A
	$I_D(T_C = 100^\circ C)$	56	A
Pulsed Drain Current ^A	I_{DM}	320	A
Maximum Power Dissipation ^B	P_D	85	W
Single Pulse Avalanche Energy	E_{AS}	308	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristic

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	45	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.5	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Gate-Threshold Voltage	$V_{th(GS)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	2	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$			1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 30\text{A}$		3.7	4.5	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$		5.3	6.8	m Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $F = 1\text{MHz}$		1970	1990	pF
Output Capacitance	C_{oss}			215	219	
Reverse Transfer Capacitance	C_{rss}			178	183	

Switching Capacitance

Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 15\text{V}, R_L = 3\Omega$ $V_{GS} = 10\text{V}, R_{GEN} = 3\Omega$		20		ns
Turn-On Rise Time	t_r			15		ns
Turn-Off Delay Time	$t_{d(off)}$			60		ns
Turn-Off Fall Time	t_f			10		ns
Total Gate Charge	Q_g	$V_{DS} = 15\text{V}, I_D = 5\text{A},$ $V_{GS} = 4.5\text{V}$		37.3		nC
Gate-Source Charge	Q_{gs}			5.8		nC
Gate-Drain Charge	Q_{gd}			7.7		nC

Drain-Source Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_D = 5\text{A}$			1.2	V
Diode Forward Current	I_S				80	A

Notes:

- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^{\circ}\text{C}$.
- The power dissipation P_D is based on $T_{J(MAX)} = 150^{\circ}\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

Typical Electrical and Thermal Characteristics

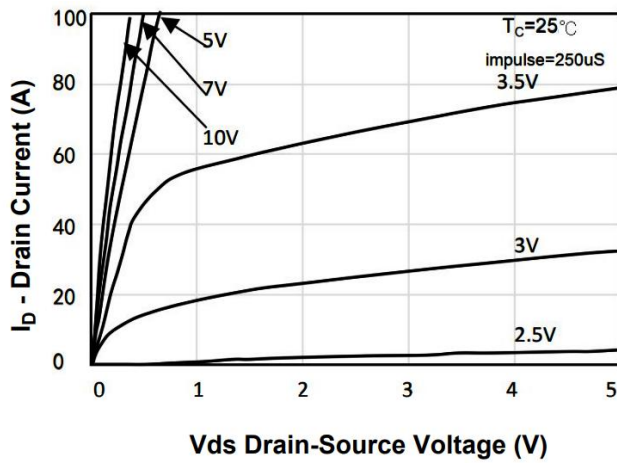


Figure 1. On-Region Characteristics

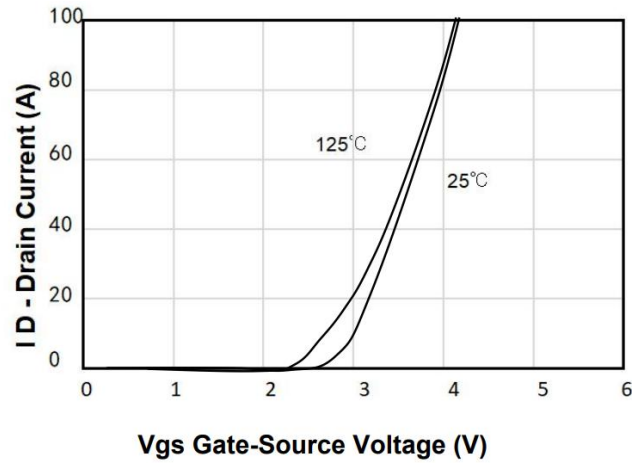


Figure 2. Transfer Characteristics

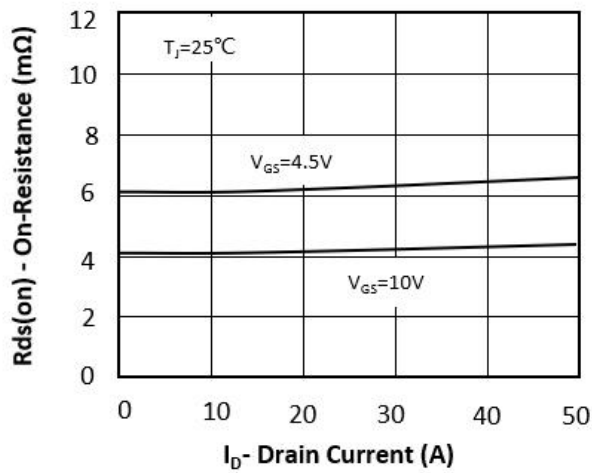


Figure 3. On-Resistance vs. Drain Current

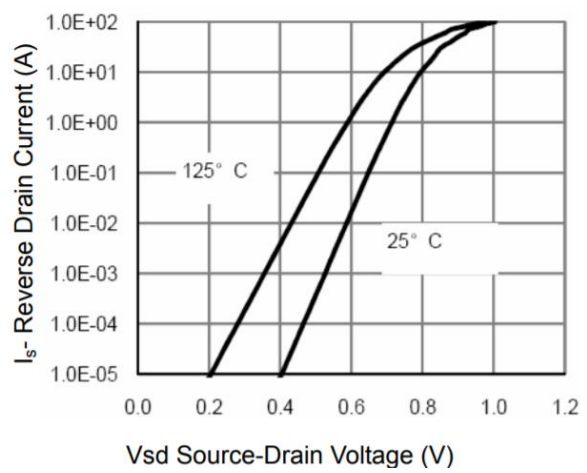


Figure 4. Body Diode Characteristics

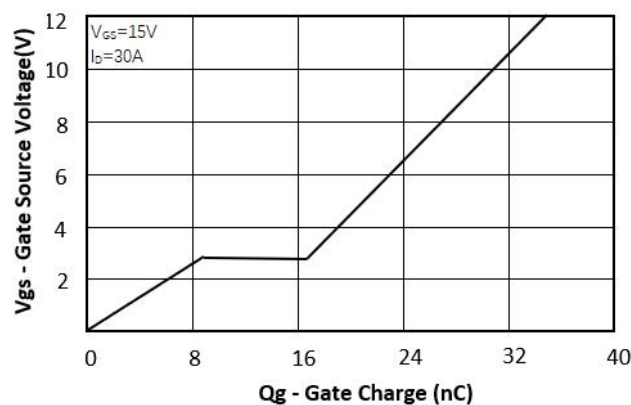


Figure 5. Gate Charge Characteristics

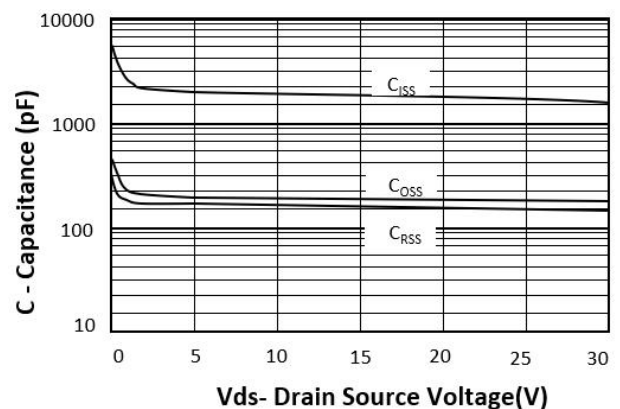


Figure 6. Capacitance Characteristics

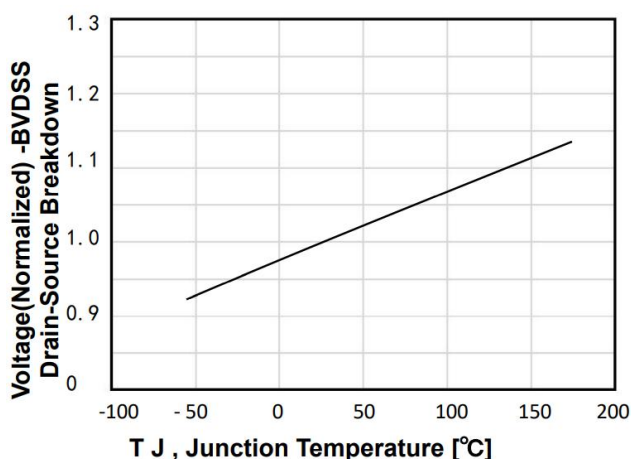


Figure 7. Breakdown Voltage Variation vs. Temperature

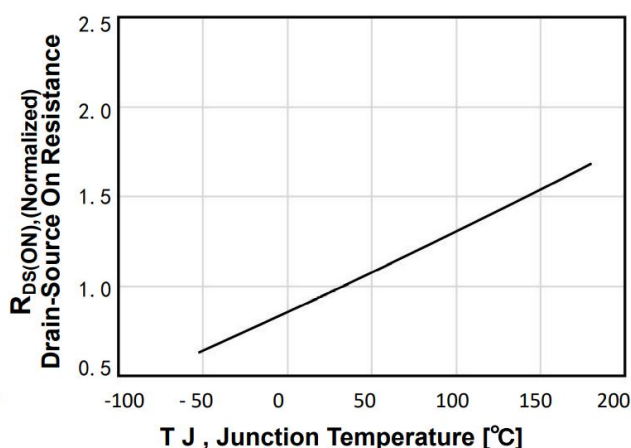


Figure 8. On-Resistance Variation vs. Temperature

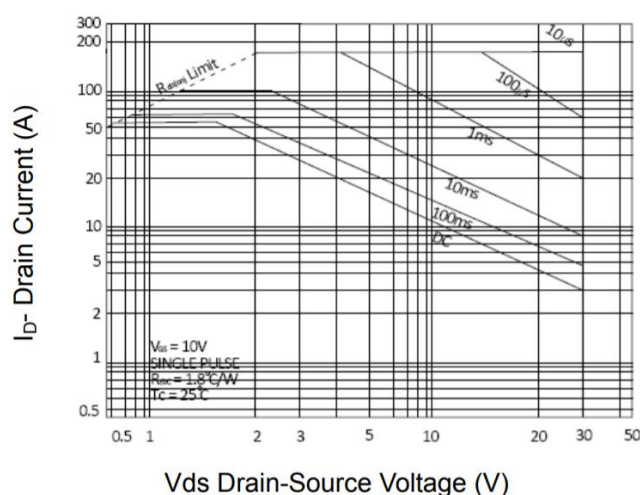


Figure 9. Safe Operation Area

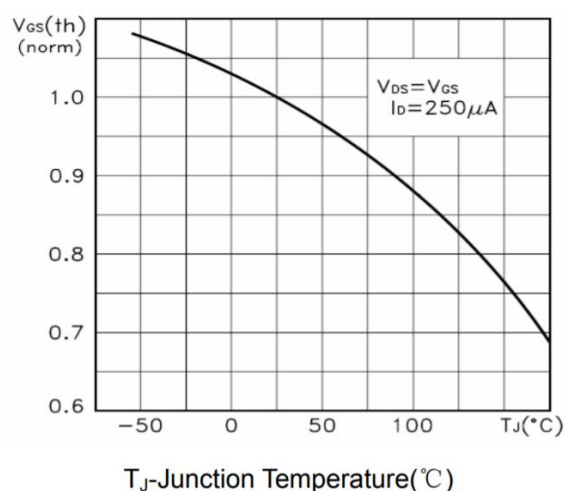


Figure 10. Current-Junction Temperature

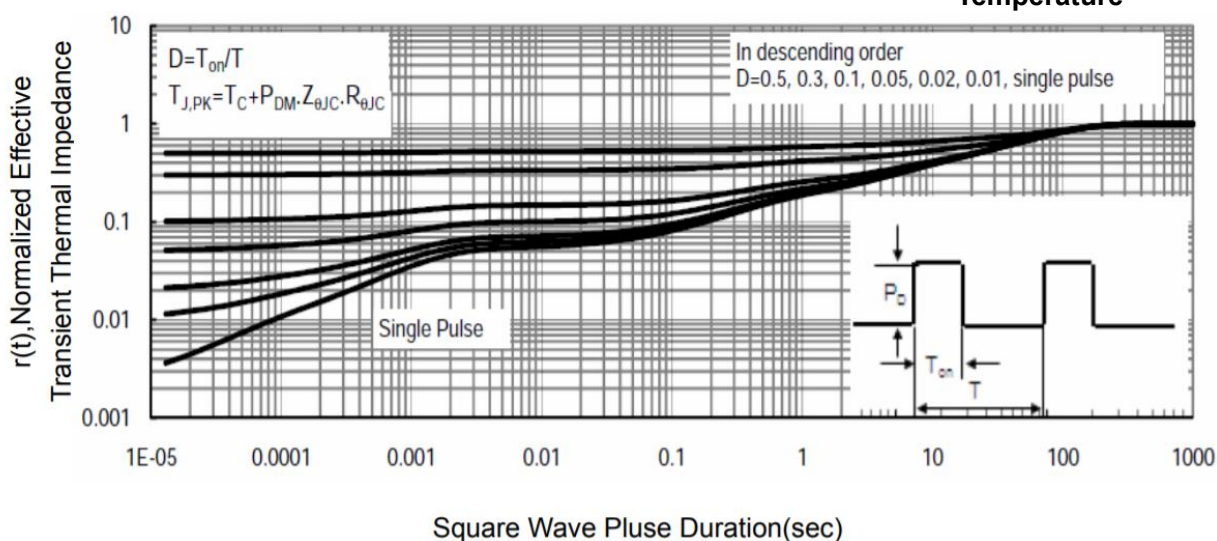


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit and Waveform

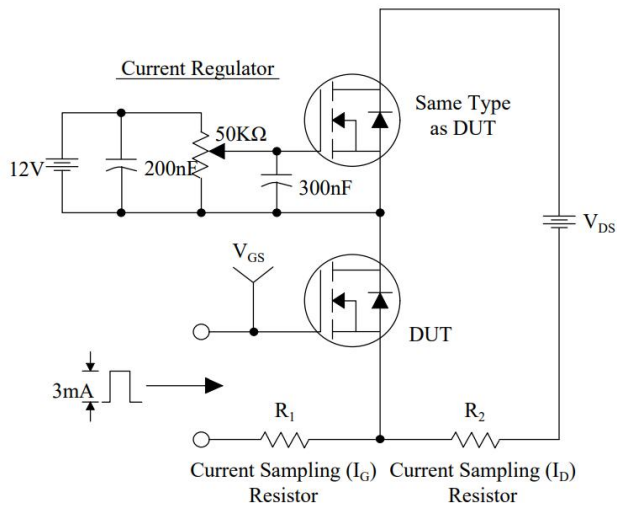


Figure 12. Gate Charge Test Circuit

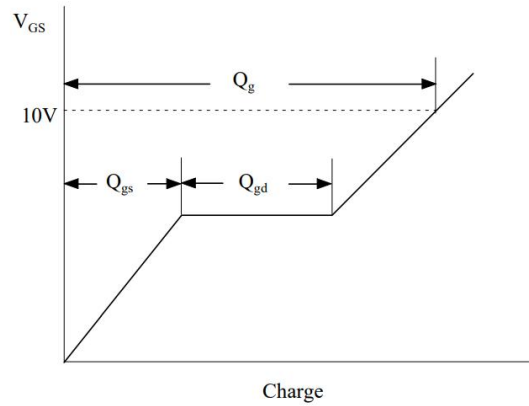


Figure 13. Gate Charge Waveform

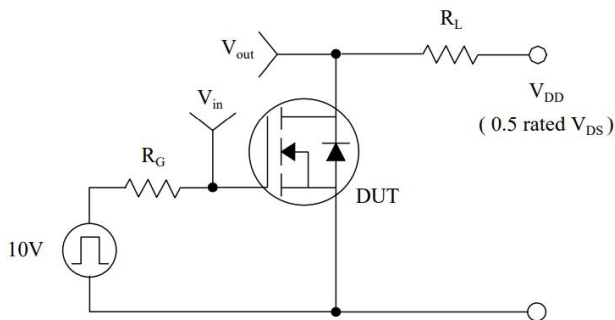


Figure 14. Resistive Switching Test Circuit

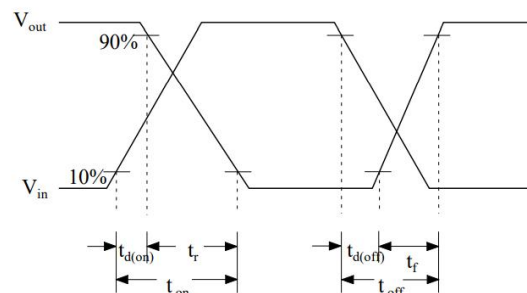


Figure 15. Resistive Switching Waveforms

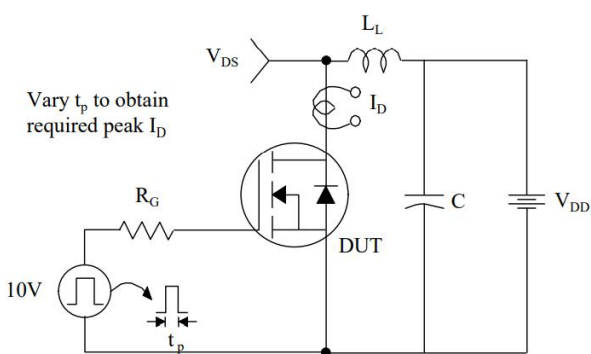


Figure 16. Unclamped Inductive Switching Test Circuit

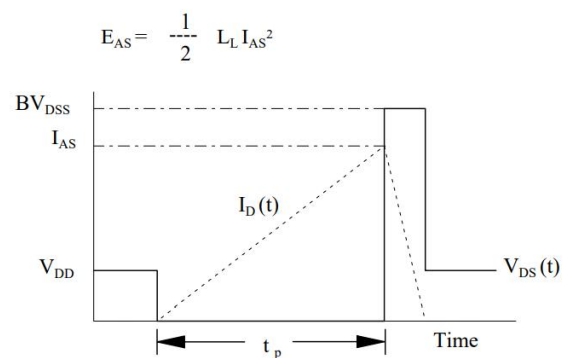
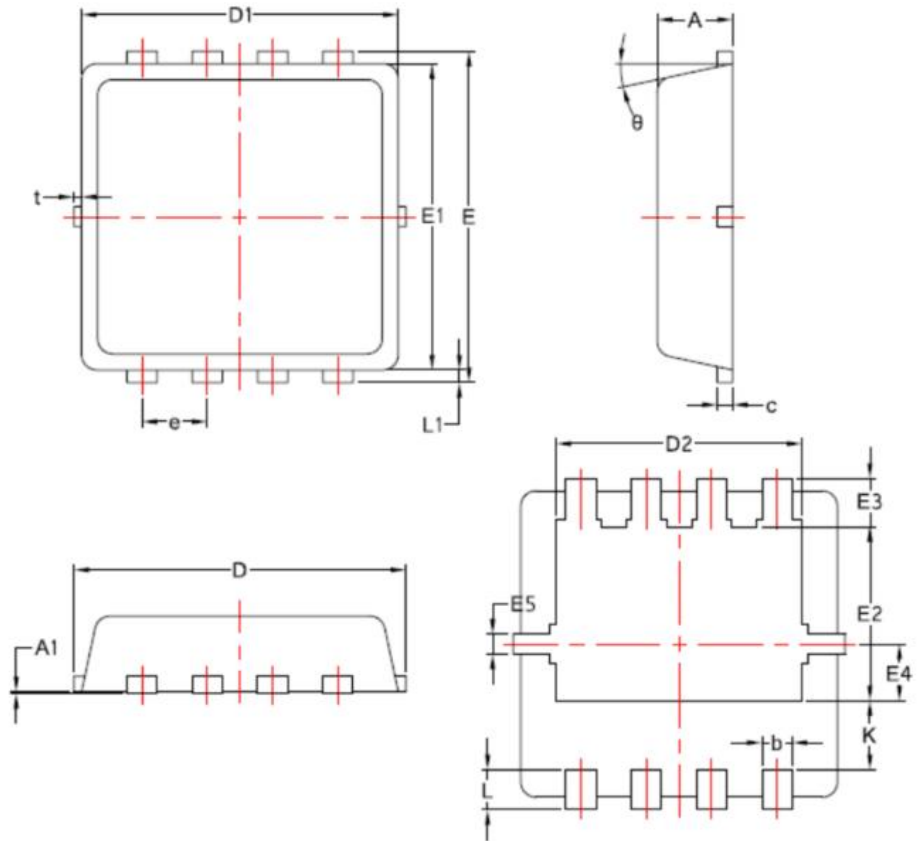


Figure 17. Unclamped Inductive Switching Waveforms

PDFN3333 Package Information

PDFN3333

SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°



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