

CHIPLINK N-Channel Enhancement Mode Power MOSFET

Description

The LX3080KA combines advanced trench technology to provide excellent $R_{DS(ON)}$, it is tailored to minimize conduction loss, and provide superior switching performance. It can be used in a wide variety of applications.

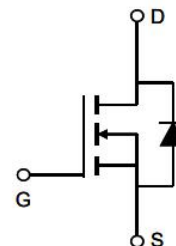
Features

- $V_{DS}=30V$, $I_D=80A$
 $R_{DS(ON)typ.}=3.9m\Omega@V_{GS}=10V$
 $R_{DS(ON)typ.}=5.8m\Omega@V_{GS}=4.5V$
- 100% Avalanche Tested
- Fast Switching
- High Power and Current Handling Capability
- Termination is Lead-free and RoHS Compliant

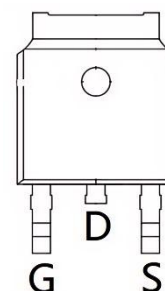


Applications

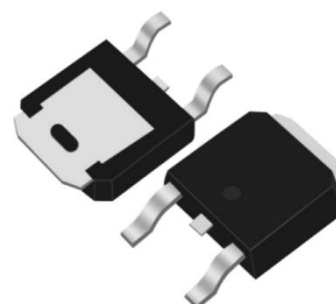
- PWM Applications
- Load Switch
- Power Management



Schematic Diagram



Pin Assignment



TO252 Package

Maximum Ratings

($T_A = 25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D (T_C = 25^\circ C)$	80	A
	$I_D (T_C = 100^\circ C)$	45	A
Pulsed Drain Current ^{BC}	I_{DM}	320	A
Maximum Power Dissipation ^{AC}	P_D	70	W
Single Pulse Avalanche Energy ^D	E_{AS}	156	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	$^{\circ}\text{C}/\text{W}$
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Electrical Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30	--	--	V
Gate-Threshold Voltage	$V_{th(GS)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.6	2.2	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	--	--	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	--	--	1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	--	3.9	4.5	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	--	5.8	7	m Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $F = 1\text{MHz}$	--	1977	--	pF
Output Capacitance	C_{oss}		--	220	--	
Reverse Transfer Capacitance	C_{rss}		--	173	--	

Switching Capacitance

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{V}, R_L = 3\Omega$ $V_{GS} = 10\text{V}, R_{GEN} = 3\Omega$	--	21	--	ns
Turn-On Rise Time	t_r		--	16	--	ns
Turn-Off Delay Time	$t_{d(off)}$		--	62	--	ns
Turn-Off Fall Time	t_f		--	9	--	ns
Total Gate Charge	Q_g	$V_{DS} = 15\text{V}, I_D = 5\text{A},$ $V_{GS} = 4.5\text{V}$	--	37	--	nC
Gate-Source Charge	Q_{gs}		--	5.6	--	nC
Gate-Drain Charge	Q_{gd}		--	8	--	nC

Drain-Source Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_D = 1\text{A}$	--	0.7	1.2	V
Diode Forward Current	I_S		--	--	80	A

Notes:

- The Power dissipation P_D is based on $T_{J(MAX)} = 150^{\circ}\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^{\circ}\text{C}$.
- The Static characteristics in Figures are obtained using $< 300\mu\text{s}$ pulses, duty cycle 2% max.
- E_{AS} condition: $T_J = 25^{\circ}\text{C}$, $V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$.

Typical Electrical and Thermal Characteristics

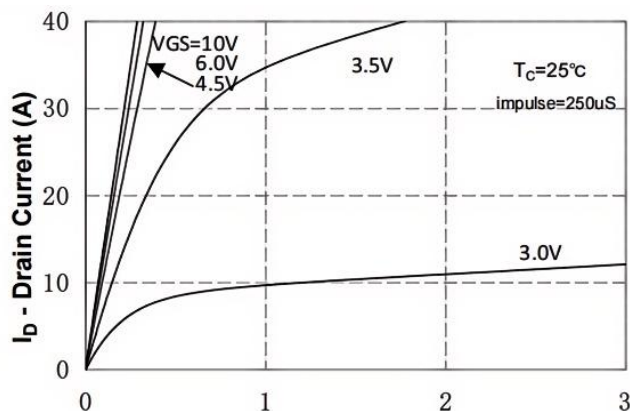


Figure 1. On Region Characteristics

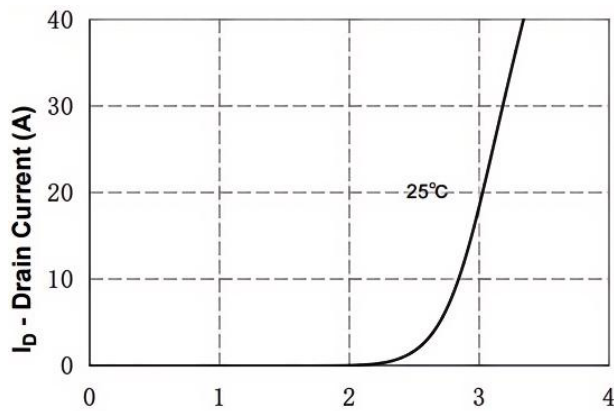


Figure 2. Transfer Characteristics

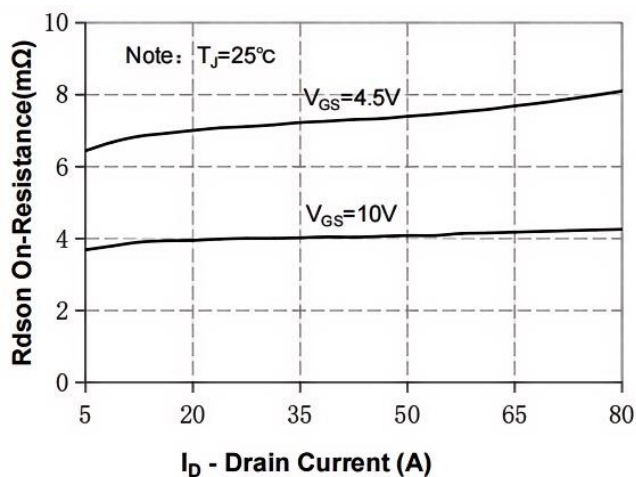


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

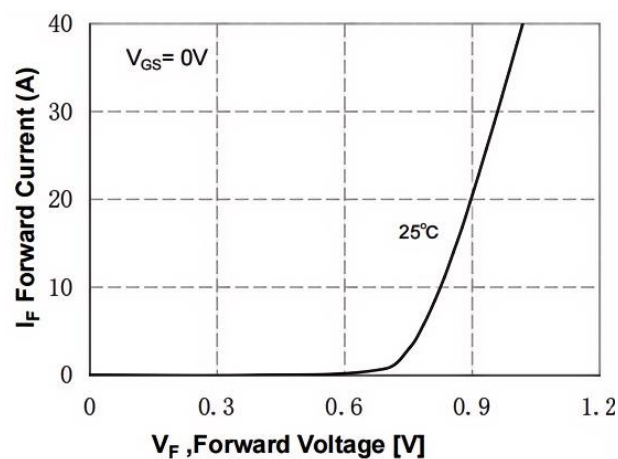


Figure 4. Body Diode Forward Voltage Variation vs. Source Current

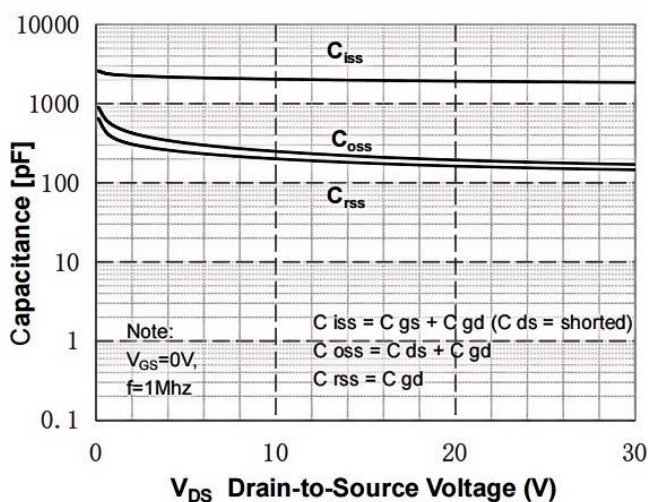


Figure 5. Capacitance Characteristics

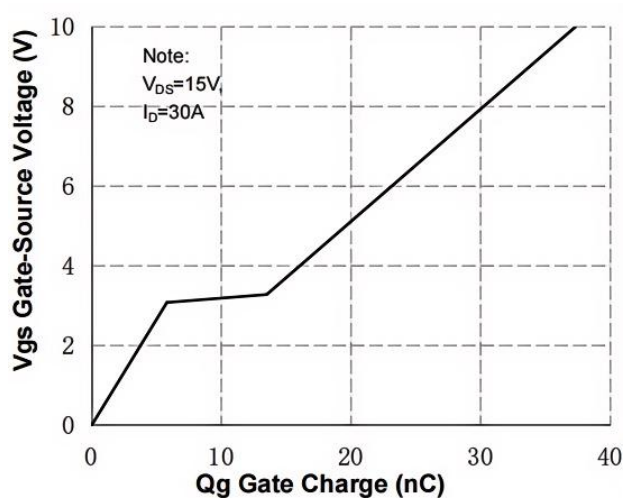


Figure 6. Gate Charge Characteristics

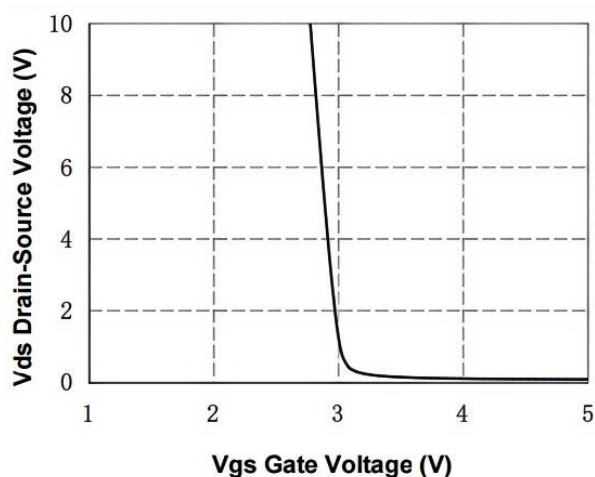


Figure 7. Vds Drain-Source Voltage vs. Gate Voltage

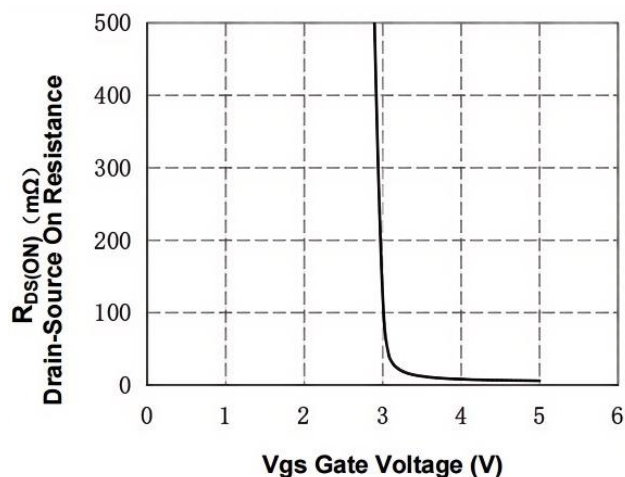


Figure 8. On Resistance vs. Gate Voltage

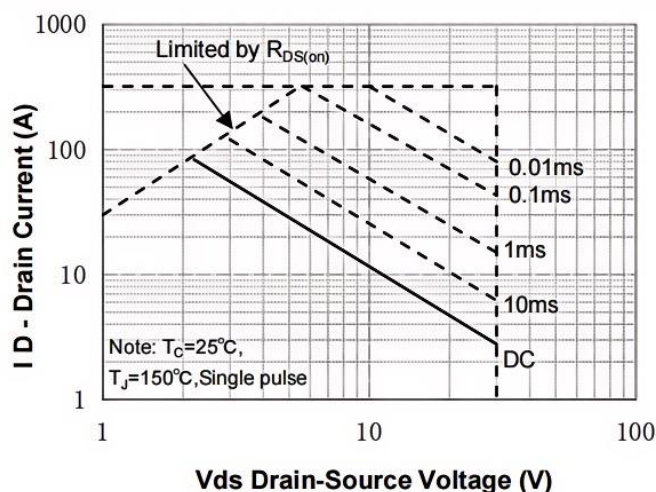


Figure 9. Maximum Safe Operating Area

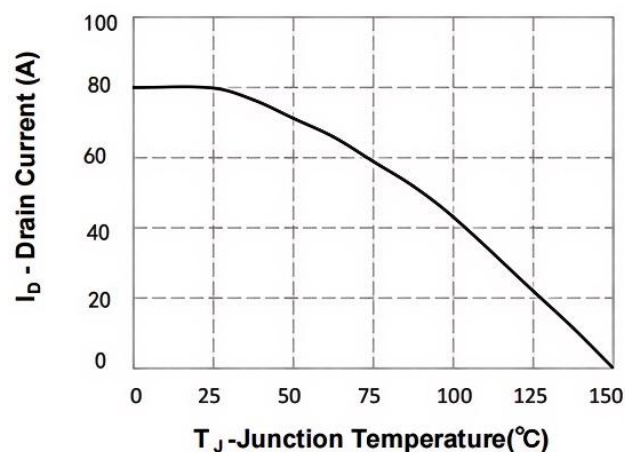


Figure 10. Maximum Continuous Drain Current vs. Temperature

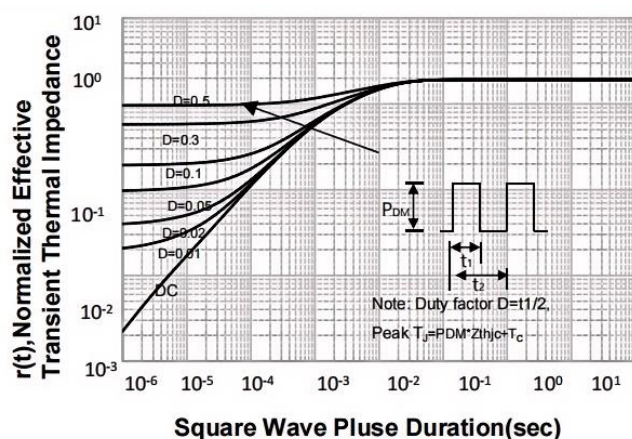


Figure 11. Transient Thermal Response Curve

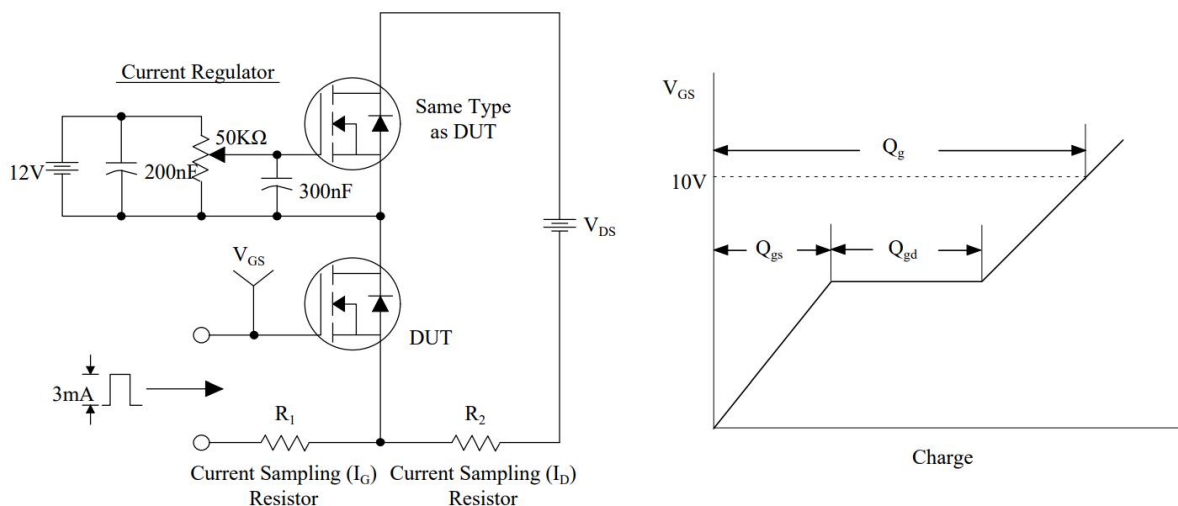


Figure 12. Gate Charge Test Circuit & Waveform

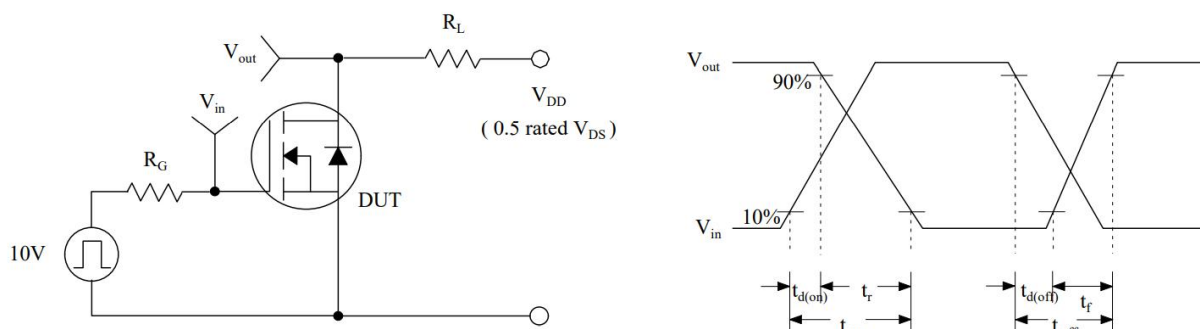


Figure 13. Resistive Switching Test Circuit & Waveforms

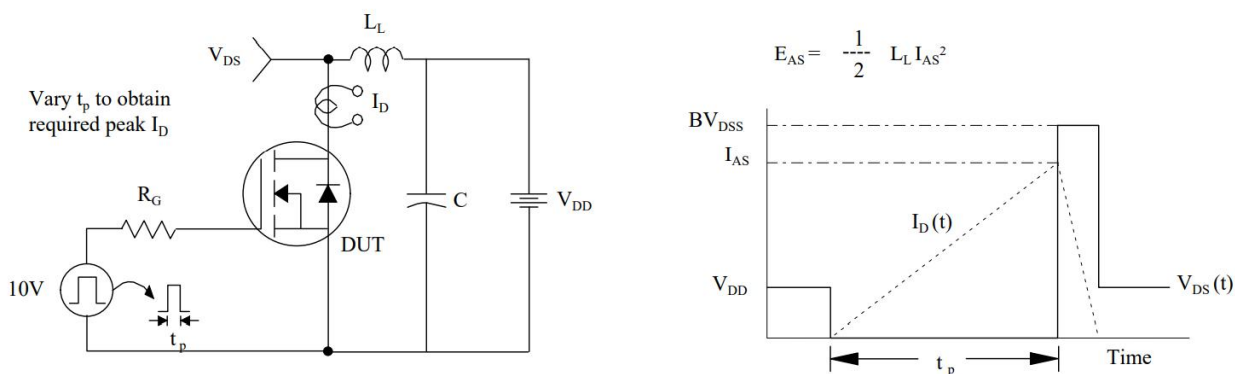
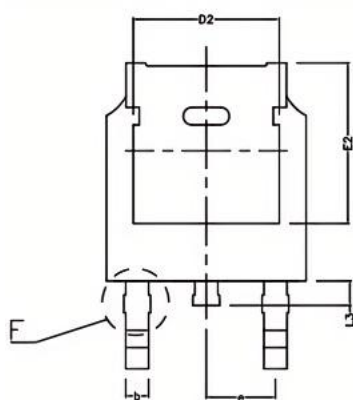
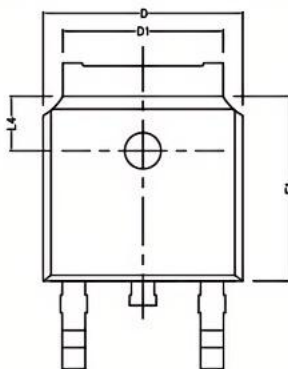


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

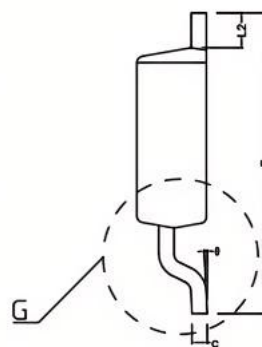
TO252 Package Information



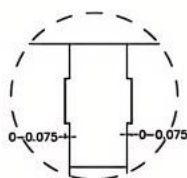
BOTTOM VIEW



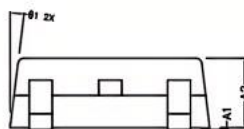
TOP VIEW



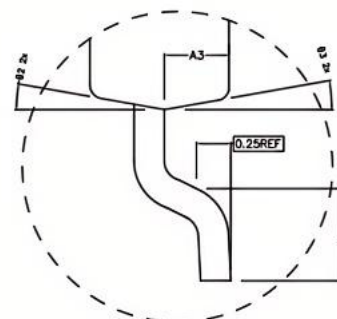
SIDE VIEW



DETAIL F



SIDE VIEW



DETAIL G

	MIN	NORMAL	MAX		MIN	NORMAL	MAX
A1	0.000	0.100	0.150	E2	5.600REF		
A2	2.200	2.300	2.400	e	2.286TYPE		
A3	1.020	1.070	1.120	L	1.400	1.550	1.700
b	0.710	0.760	0.810	L2	1.10REF		
c	0.460	0.508	0.550	L3	0.80REF		
D	6.500	6.600	6.700	L4	1.8REF		
D1	5.330REF			θ	0~8°		
D2	4.830REF			θ1	7° TYPE		
E	9.900	10.100	10.300	θ2	10° TYPE		
E1	6.000	6.100	6.200	θ3	10° TYPE		

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