

CH IPLINK N-Channel Enhancement Mode Power MOSFET

Description

The LX3060K combines advanced trench technology to provide excellent $R_{DS(ON)}$, it is tailored to minimize conduction loss, and provide superior switching performance. It can be used in a wide variety of applications.

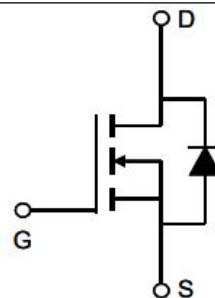
Features

- $V_{DS}=30V$, $I_D=60A$
 $R_{DS(ON)typ.}=5.8m\Omega@V_{GS}=10V$
 $R_{DS(ON)typ.}=10m\Omega@V_{GS}=4.5V$
- Fast Switching
- High Power and Current Handling Capability
- Termination is Lead-Free and RoHS Compliant

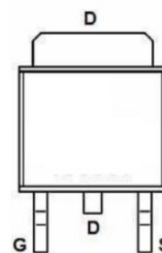


Applications

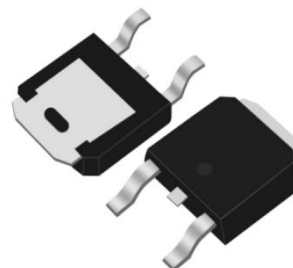
- PWM Applications
- Load Switch
- Power Management



Schematic Diagram



Pin Assignment



TO252 Package

Maximum Ratings

($T_A = 25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D(T_C=25^\circ C)$	60	A
	$I_D(T_C=100^\circ C)$	40	A
Pulsed Drain Current ^{BC}	I_{DM}	92	A
Maximum Power Dissipation ^A	P_D	29	W
Single Pulse Avalanche Energy ^D	E_{AS}	58	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristic

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.32	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Gate-Threshold Voltage	$V_{th(GS)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	2.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$			1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 25\text{A}$		5.8	7.5	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 15\text{A}$		10	14	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{V}, I_D = 15\text{A}$	10			S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $F = 1\text{MHz}$		1140		pF
Output Capacitance	C_{oss}			175		
Reverse Transfer Capacitance	C_{rss}			151		

Switching Capacitance

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{V}, I_D = 5\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 3.3\Omega$		15		ns
Turn-On Rise Time	t_r			19		ns
Turn-Off Delay Time	$t_{d(off)}$			35		ns
Turn-Off Fall Time	t_f			21		ns
Total Gate Charge	Q_g	$V_{DS} = 15\text{V}, I_D = 5\text{A},$ $V_{GS} = 4.5\text{V}$		9.2		nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			5		nC

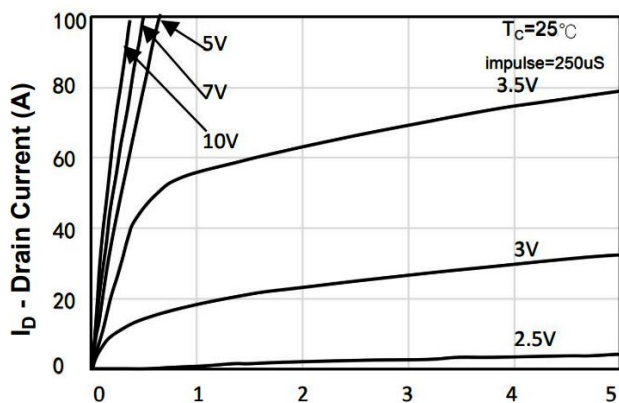
Drain-Source Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_D = 5\text{A}$			1.2	V
Diode Forward Current	I_S				60	A

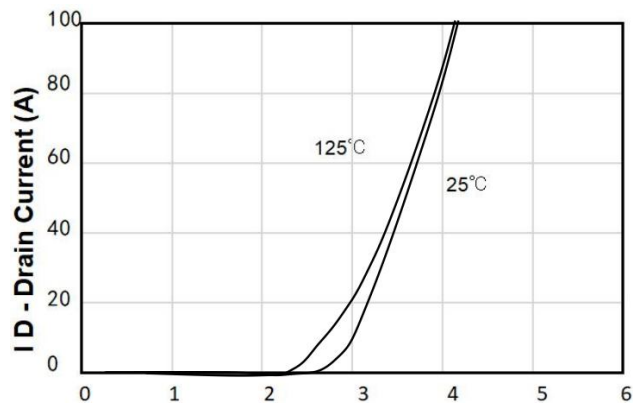
Notes:

- The Power dissipation P_D is based on $T_{J(MAX)} = 150^{\circ}\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^{\circ}\text{C}$.
- The Static characteristics in Figures are obtained using $< 300\mu\text{s}$ pulses, duty cycle 2% max.
- E_{AS} condition: $T_J = 25^{\circ}\text{C}$, $V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$, $L = 0.1\text{mH}$.

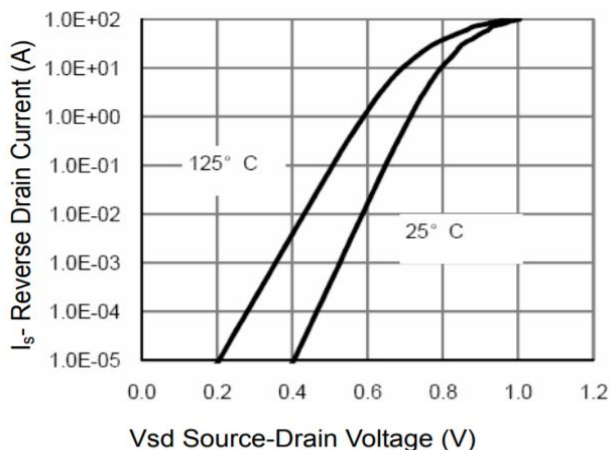
Typical Electrical and Thermal Characteristics



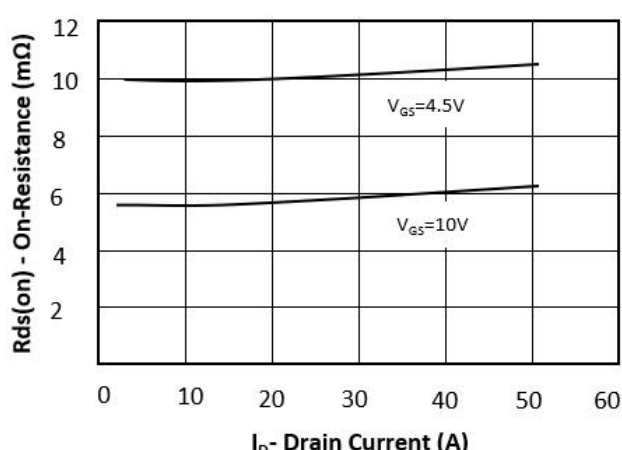
Vds Drain-Source Voltage (V)
Figure 1. On-Region Characteristics



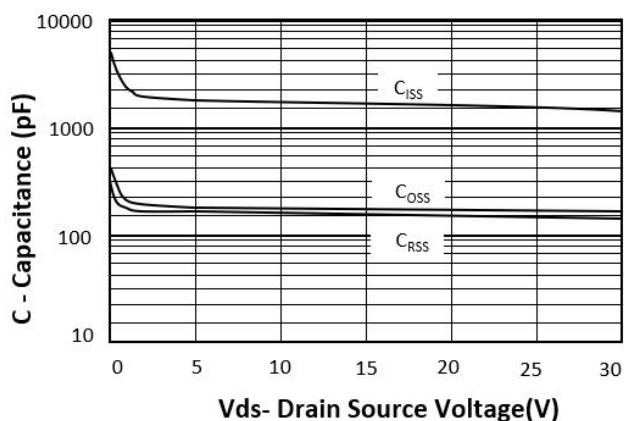
Vgs Gate-Source Voltage (V)
Figure 2. Transfer Characteristics



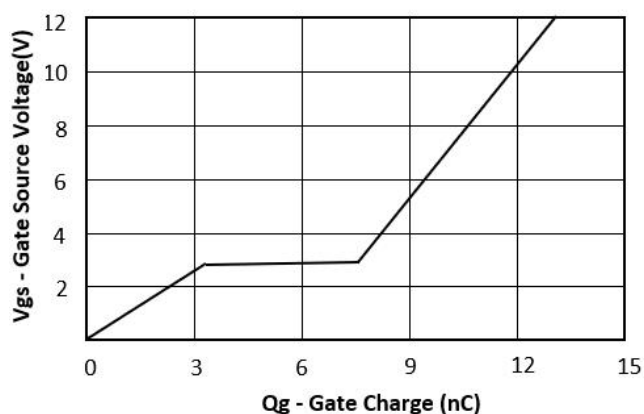
Vsd Source-Drain Voltage (V)
Figure 3. Body Diode Characteristics



ID- Drain Current (A)
Figure 4. On-Resistance vs. Drain Current



Vds- Drain Source Voltage(V)
Figure 5. Gate Charge Characteristics



QG - Gate Charge (nC)
Figure 6. Capacitance Characteristics

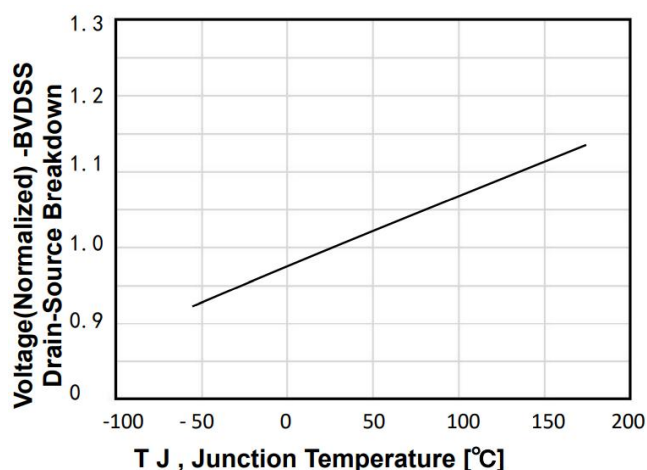


Figure 7. Breakdown Voltage vs. Temperature

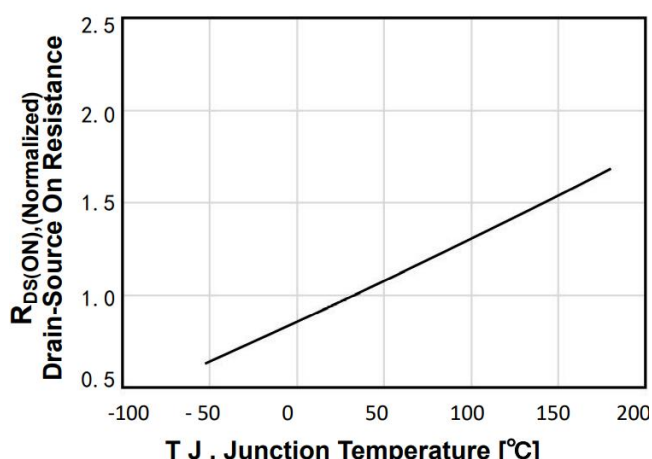


Figure 8. On-Resistance Variation vs. Temperature

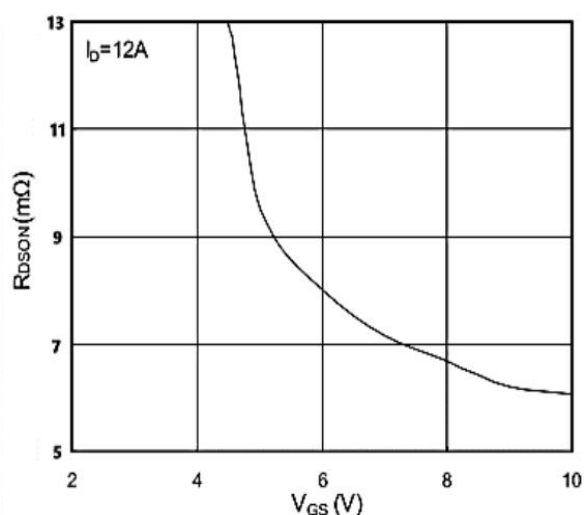


Figure 9. On-Resistance vs. VGS

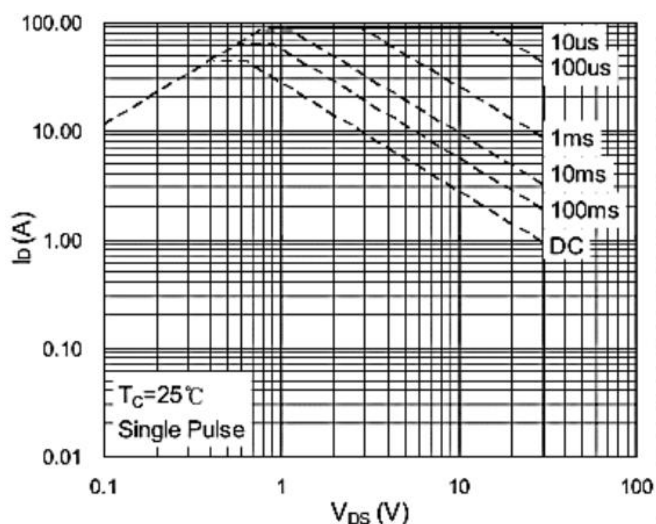


Figure 10. Safe Operation Area

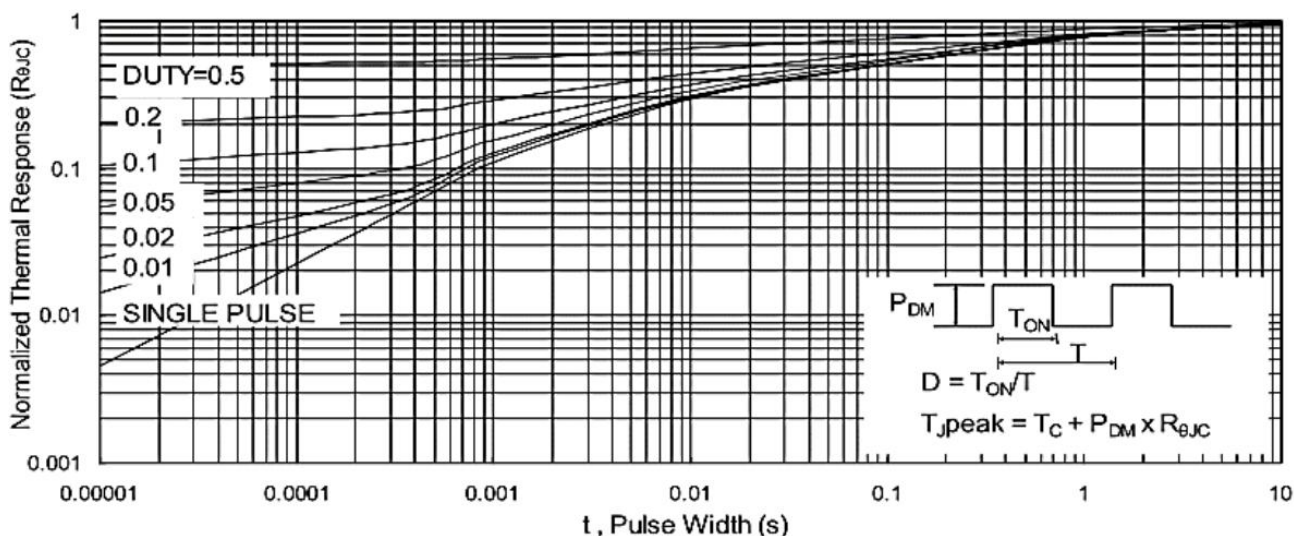


Figure 11. Normalized Maximum Transient Thermal Impedance

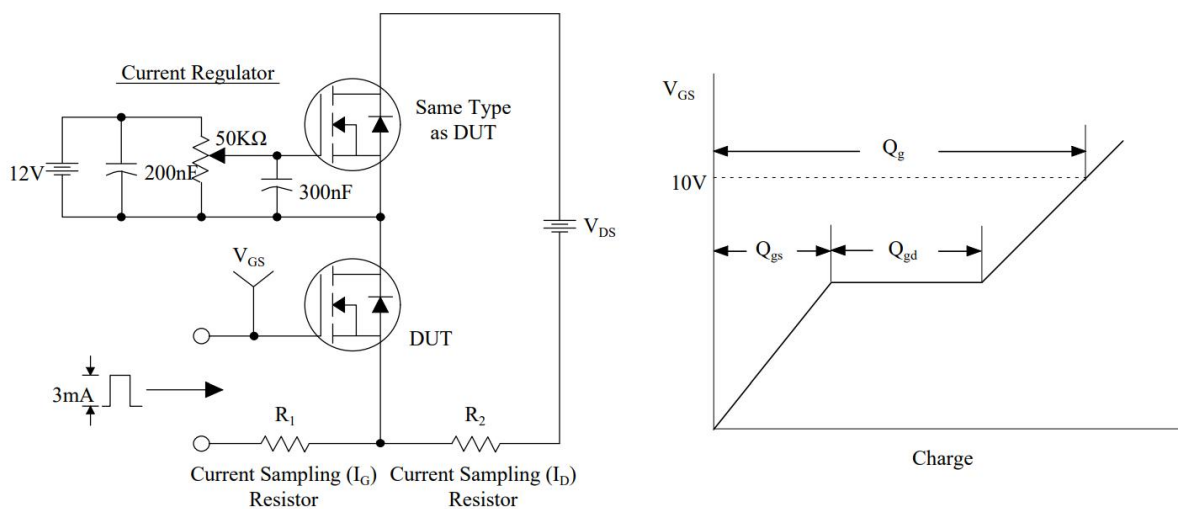


Figure 12. Gate Charge Test Circuit & Waveform

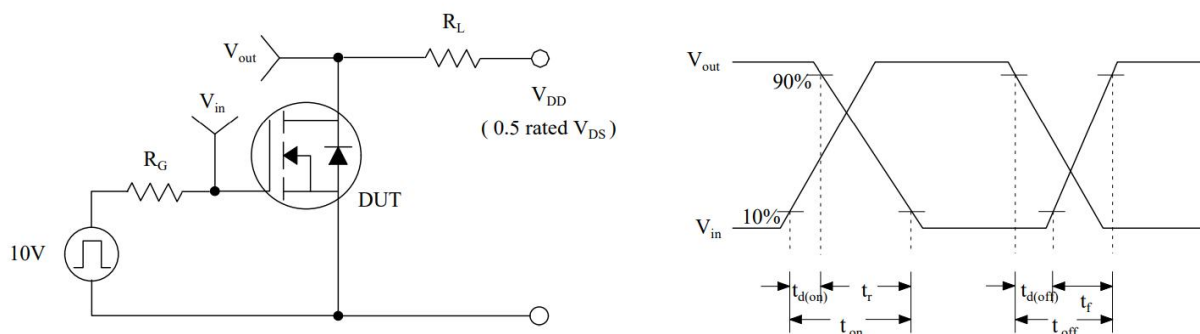


Figure 13. Resistive Switching Test Circuit & Waveforms

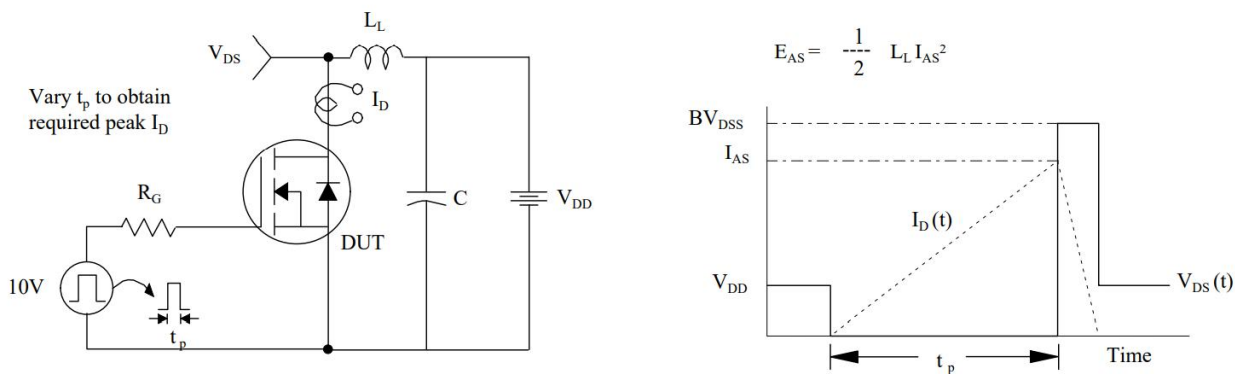
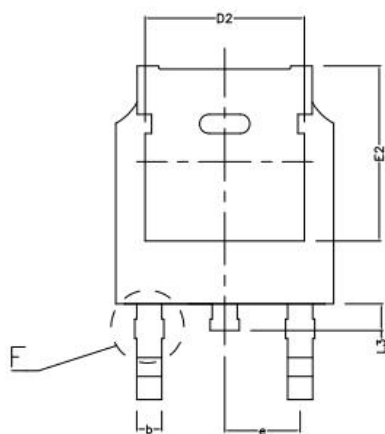
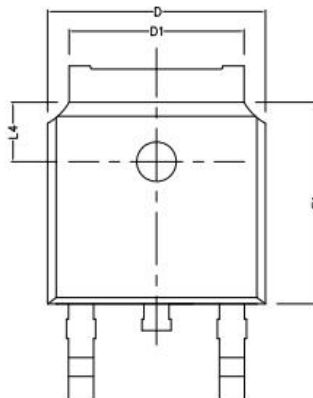


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

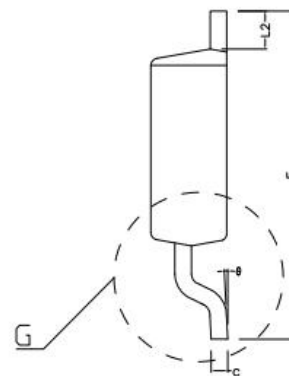
TO252 Package Information



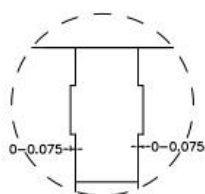
BOTTOM VIEW



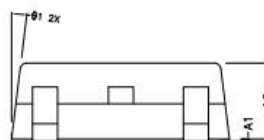
TOP VIEW



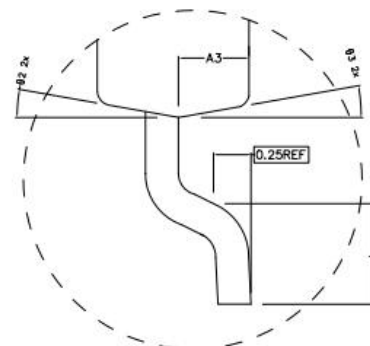
SIDE VIEW



DETAIL F



SIDE VIEW



DETAIL G

	MIN	NORMAL	MAX		MIN	NORMAL	MAX
A1	0.000	0.100	0.150	E2	5.600REF		
A2	2.200	2.300	2.400	e	2.286TYPE		
A3	1.020	1.070	1.120	L	1.400	1.550	1.700
b	0.710	0.760	0.810	L2	1.10REF		
c	0.460	0.508	0.550	L3	0.80REF		
D	6.500	6.600	6.700	L4	1.8REF		
D1	5.330REF			θ	0~8°		
D2	4.830REF			θ1	7° TYPE		
E	9.900	10.100	10.300	θ2	10° TYPE		
E1	6.000	6.100	6.200	θ3	10° TYPE		

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