ITE7655BA

COT Mode, 5A, 2.5~6.0V, Synchronous, 1.2MHz, Step-Down DC/DC Converters

Features

- Wide 2.5V to 6.0V Operating Input Range
- 5A Continuous Output Current
- 1.2MHz Switching Frequency
- Short Protection with Hiccup-Mode
- Built-in Overcurrent Limit
- PFM for High Efficiency in Light Load Condition
- Integrated Internal Soft-Start
- 52/37mΩ Low RDS(ON) Internal MOSFETS
- Output Adjustable from 0.6V
- Low EMI Signature
- 100% Duty Cycle
- Built-in 35Ω Discharge Resistor
- Thermal Shutdown
- COT Mode
- MSL3 Package Level

Applications

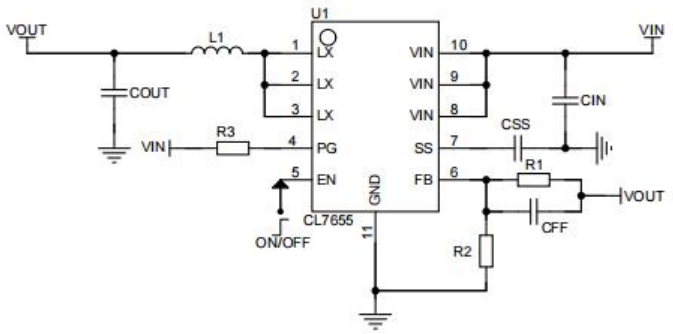
- Automotive Entertainment
- Wireless and DSL Modems
- Digital Still and Video Cameras
- Portable Instruments
- SSD

Description

The ITE7655BA is a high-efficiency monolithic synchronous buck regulator using a constant frequency, COT mode architecture. The device is available in an adjustable version.Supply current with no load is 35uA and drops to <1uA in shutdown. The 2.5V to 6.0V input voltage range makes the ITE7655BA ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, ITE7655BA extending battery life in portable systems.PFM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 1.2MHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

The requires a minimal number of readily available, external components and is available in a small package.

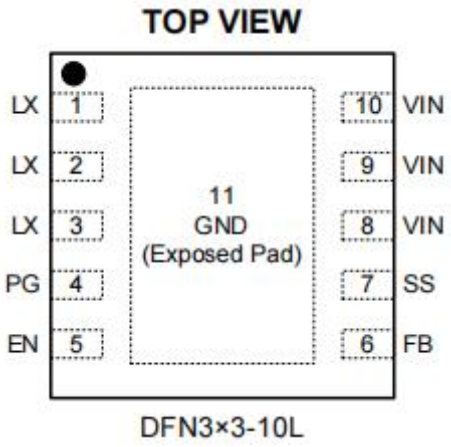
Simplified Application Circuit



Marking Information

Y : Year
W: Week
LL: Lot Number

Pin Configuration



DFN3×3-10L

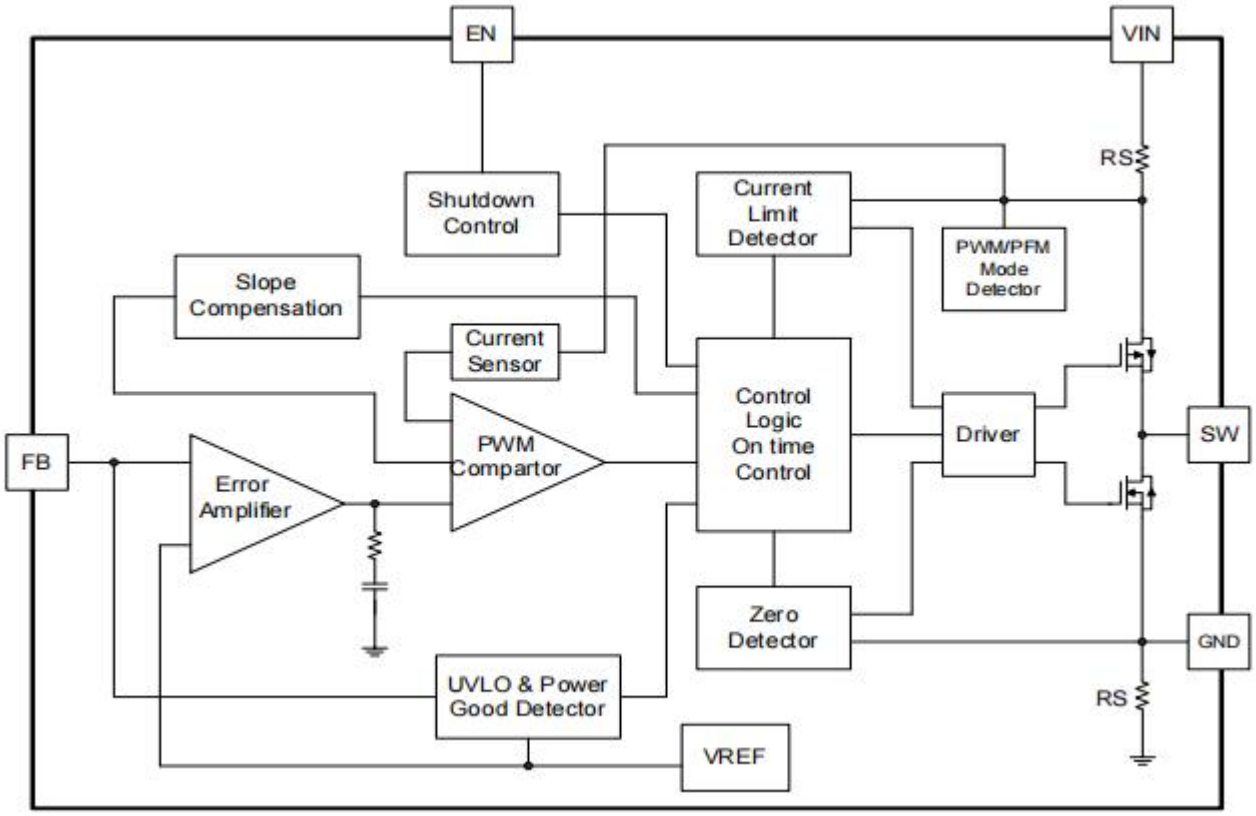
Pin Description

NO.	NAME	FUNCTION
1/2/3	LX	Power switch output. It is the switch node connection to inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
4	PG	Power good indicator (Open drain output). Low if the output<90% of regulation voltage or >120% of regulation voltage; high otherwise. Connect a pull-up resistor (100KΩ) to the input.
5	EN	Chip enable pin. Drive EN above 1.0V to turn on the part. Drive EN below 0.4V to turn it off. Do not leave EN floating.
6	FB	Output voltage feedback pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
7	SS	Soft-start programming pin. Connect a capacitor from this pin to ground to program the soft-start time. Css/100nF=6mS.
8/9/10	VIN	Power supply input.
11	GND	Ground pin.

Order Information

PART NO.	PRODUCT DESCRIPTION
ITE7655BA	B: OVP A: PFM

Functional Block Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	RANGE	UNIT
VIN Voltage	V_{IN}	-0.3 ~ 6.5	V
EN Voltage	V_{EN}	-0.3 ~ 6.5	V
SW Voltage	V_{SW}	-3 (<10nS) ~ VIN + 1.5 (<10nS)	V
FB Voltage	V_{FB}	-0.3 ~ 6.5	V
Power Dissipation (3)	/	Internally Limited	/
Operating Junction Temperature,TJ	T_J	-40 ~ +150	℃
Storage Temperature, Tstg	T_{stg}	-65 ~ +150	℃
Lead Temperature (Soldering, 10sec.)	T_{solder}	260	℃

Note(1): Exceeding these ratings may damage the device.
Note(2): The device is not guaranteed to function outside of its operating conditions

Recommended Operating Conditions

PARAMETER	RANGE	UNIT
Operating Junction Temperature (1)	-40 ~ 125	℃
Operating Temperature Range	-40 ~ 85	℃
Input Voltage VIN	2.5 ~ 5.5	V
Output Current	0 ~ 5	A

Note(1): All limits specified at room temperature (TA = 25℃) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

PARAMETER	DESCRIPTION	DFN3*3-10L	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1)(2)	43	℃/W
$R_{\theta JC(top)}$	Junction-to-Case (top) Thermal Resistance	46	℃/W

Note(1): The package thermal impedance is calculated in accordance to JESD 51-7.
Note(2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

ESD Ratings

PARAMETER	DESCRIPTION	VALUE	UNIT
HBM	Human-Body Model, pre ANS/ESDA/JEDEC JS-001	±2000	V
CDM	Charge-Device Model, pre ANS/ESDA/JEDEC JS-002	±1000	V

Electrical Characteristics

VIN=5V, TJ=25℃, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		2.5		5.5	V
OVP Threshold				6.5		V
V_{IN_UVLO}	VIN Under-Voltage Lockout Threshold			2.5	2.8	V
V_{IN_HYS}	VIN Under-Voltage Lockout Threshold-Hysteresis			300		mV
I_Q	Quiescent Current into VIN	V_{IN}=5V, V_{OUT}=1.8V, I_{LOAD}=0A		35	55	μA
I_{SD}	Shutdown Current into VIN Pin	V_{EN}=0V, V_{IN}=5V			1	μA
V_{FB}	Regulated Feedback Voltage	V_{IN}=5V, T_J=25℃	0.59	0.6	0.61	V
$\triangle V_{LINE\_VIN}$	Output Voltage Line Regulation	V_{IN}=2.5V to 6V			0.5	%
$\triangle V_{LOAD}$	Output Voltage Load Regulation	V_{IN}=5V, Vout=1.8V, Δ_{VLOAD}(0-5A)			1	%
fsw	Oscillation Frequency 1	V_{IN}=5V, Vout=1.8V, I_{LOAD}=1A	0.7	1.2	1.4	MHz
R_{DSON}	ON Resistance of PMOS	I_{SW}=100mA		52		mΩ
R_{DSON}	ON Resistance of NMOS	I_{SW}=-100mA		37		mΩ
IL_{IMIT}_H	High-Side Switch Current Limit	V_{IN}=5V, FB=90%		8.4		A
IL_{IMIT}_L	Low-Side Switch Current Limit	V_{IN}=5V, FB=90%		6.3		A
V_{EN_H}	EN Rising Threshold		1.5			V
V_{EN_L}	EN Falling Threshold				0.4	V
V_{EN_HYS}	EN Threshold Hysteresis			100		mV
I_{EN}	EN Leakage Current				1	μA
I_{SW}	SW Leakage Current	V_{EN}=0V, V_{IN}=V_{SW}=5V			1	μA
T_{SS}	Soft Start	CSS=100nF		6		ms
		Without Css		0.6		ms
R_{DIS}	Output Discharger Resistance	V_{IN}=5V, EN=0V		35		Ω
T_{SD}	Thermal Shutdown			160		℃
T_{SD_HYS}	Thermal Hysteresis			10		℃

Functions Description

Internal Regulator

The ITE7655BA is a COT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.2MHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160℃ , it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 150℃) , the chip is enabled again.

SS (Power Start)

The ITE7655BA provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor between SS pin and GND. The chip provides a 10μA charge current for the external capacitor. If a 0.1μF capacitor is used to set the soft-start, its period will be 6ms. If set this to NC, the soft-start time will be 0.6ms. The calculations for the slow-start time and slow-start capacitor are shown in the next equation:

$$\mathrm{Tss} = \frac{C_{SS} \times V_{REF}}{I_{SS}}$$

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If VFB is greater than VPG, R and less than VOVP for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to VIN or another voltage source through a resistor (e.g., 10kΩ to 100kΩ).

Applications Information

Setting the Output Voltage

ITE7655BA requires an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. ITE7655BA is internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

Example of Resistor Selection

VOUT(V)	R1(KΩ)	R2(KΩ)	L1(μH)	CIN(μF)	COUT(μF)	CFF (pF) Opt.
1.0	6.67	10	1.0uH	22	22*2	10-200pF
1.5	15.00	10	1.0uH	22	22*2	10-200pF
3.3	45.00	10	2.2uH	22	22*2	10-200pF

Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current. Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25℃, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and more than 47μF or 2*22μF capacitance.

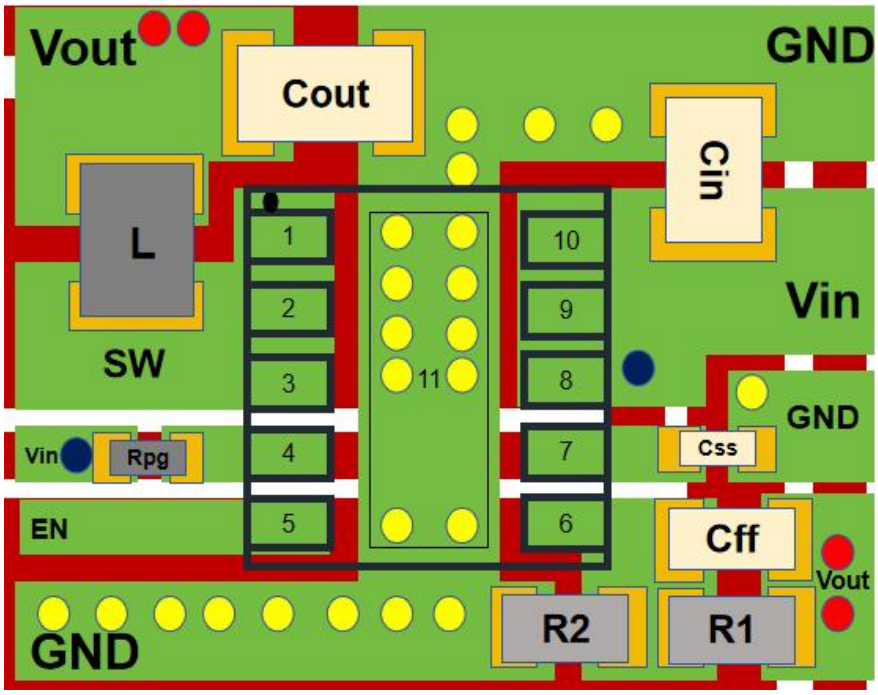
Selecting the Input Capacitor

CIN The ripple current through input capacitor is calculated as：

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor with 6.3V rating should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 22μF low ESR ceramic capacitor is recommended.

PCB Layout Example & Guidelines



The PCB layout is an important step to maintain the high performance of the ITE7655BA device.

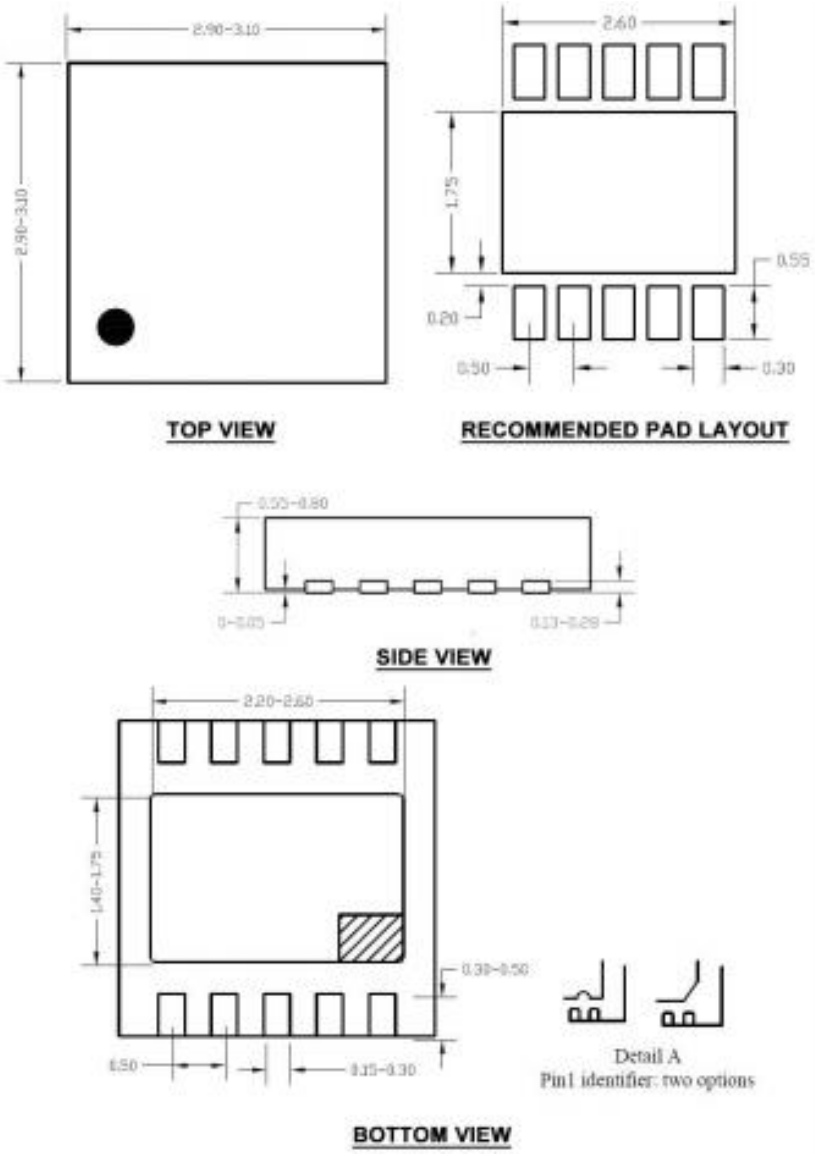
1.The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.

2. The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.

3. The sense traces connected to FB are signal traces. Special care should be taken to avoid noise beinginduced. Keep these traces away from SW nodes.

4. GND layers might be used for shielding.

Package Information: DFN3*3-10L



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

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