CL7172

6.5V,2A, Ultralow Noise, High PSRR, Fast Transient Response CMOS LDO

Description

The CL7172 is a CMOS linear regulator(LDO). It is featuring low output voltage noise, High PSRR, low dropout voltage and fast transient response. It guarantees delivery of 2A output current, and it is available in adjustable and fixed output voltage options: 1.2V~5.0V.

Based on its high output current, low output noise and excellent line and load transient response, the CL7172 is ideal for high performance noise sensitive analog and mixed signal applications. The high power supply rejection ratio of the CL7172 holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic captive loads (4.7μF typical).

Features

- 2A output current
- Adjustable and fixed output voltage options: 1.2V to 5V
- ±1.5% Initial voltage accuracy
- Operating input voltage range: 2.3V to 6.5V
- Ultra low dropout voltage 200mV @ 2A
- Low noise: 5uVrms independent of output voltage at 100Hz to 100KHz
- Fast Transient Response:1.5us Response time for 1mA to 1.5A load step
- High PSRR: 60dB PSRR at 100KHz
- Over-circuit protection
- Short-circuit protection
- Over-temperature protection
- Build in selectable internal and external soft start

Applications

- Noise Sensitive Circuits: ADC and DAC
- Precision Amplifiers
- Clock Applications: PLLs and VOCs
- Communications Systems
- Medical and Healthcare
- Industrial Instrument

Typical Application

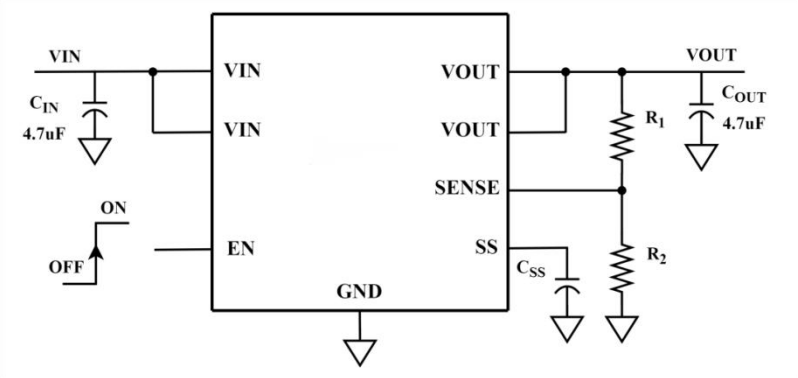


Figure 1 Typical Application of CL7172

Pin Description

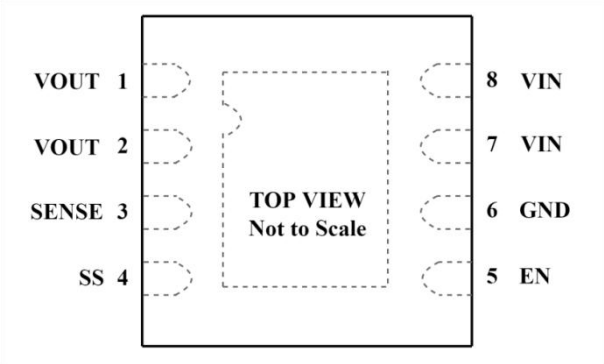


Figure 2 DFN 3×3-8L package

NO.	NAME CL7172	DESCRIPTION
1,2	VOUT	IC output voltage. Bypass this pin to GND with a minimum 4.7uF capacitor as close as possible
3	SENSE	Sense input pin. SENSE voltage is set to be 1.2V. The output voltage can be expressed by the equation: $\mathrm{VOUT} = \frac{1.2\mathrm{V}}{\mathrm{R2}} \times (\mathrm{R1} + \mathrm{R2})$
4	SS	Soft start. A 1nF external capacitor connected to SS results in a 1.0 ms start-up time.
5	EN	Enable pin, active high
6	GND	IC ground.
7,8	VIN	IC power supply. Bypass this pin to GND with a minimum 4.7uF capacitor as close as possible
9	EXP	Exposed GND pad.

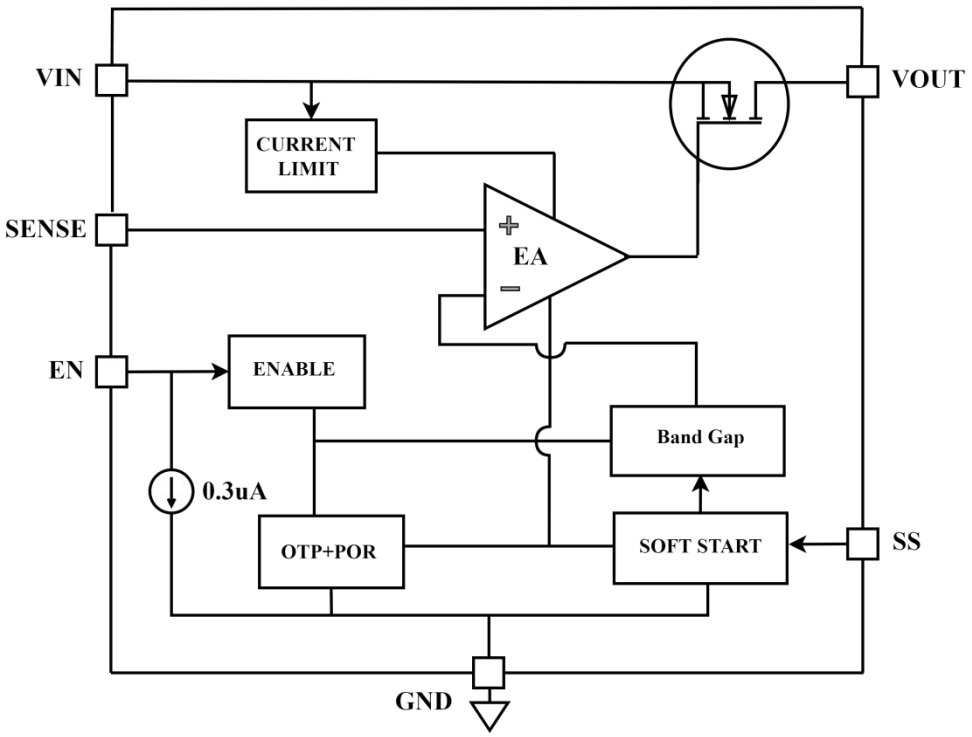
Order Information

PART NUMBER	VOUT
CL7172	ADJ/Fixed

Marking Information

PART NUMBER	PACKAGE TYPE	MARKING	DESCRIPTION
CL7172A8F	DFN 3×3-8L	dO XX	First row: d: Model code O: Voltage code Second row: Production cycle

Function Block Diagram



Absolute Maximum Ratings (Note 1)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage to GND	VIN	-0.3 < V_{IN}< 7	V
Output Voltage to GND	VOUT	-0.3 < V_{OUT}<VIN	V
EN to GND	EN	-0.3 < V_{EN}< 7	V
SS to GND	SS	-0.3 < SS<V_{IN}	V
SENSE to GND	SENSE	-0.3 < SENSE< 7	V
Package Power Dissipation at TA≦25°C	$P_{D\_DFN3\times3}$		mW
Operating Temperature	T_{opr}	-40 ~ +125	℃
Storage Temperature	T_{stg}	-65 ~ +150	℃
Soldering Temperature Soldering Time	T_{solder}	260℃, 10s	℃
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}		V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}		V

Thermal Information (Note 3)

PARAMETER	SYMBOL	LIMITS	UNIT
Thermal Resistance Junction to Ambient	θ_{JA}		℃/W
Thermal Resistance Junction to Case	θ_{JC}		℃/W

Recommended Operating Condition (Note 4)

PARAMETER	SYMBOL	LIMITS	UNIT
VIN to GND	VIN	2.3 to 6.5	V
Junction Temperature	T_J	- 40 ~ 125	℃
Operating Temperature Range	T_A	-40 ~ 85	℃

EC Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, T_A = 25℃, C_{IN}=1uF, C_{OUT}=1uF, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		2.3		6.5	V
Load Current (note 5)	I_{LOAD}				2.0	A
Operating Supply Current	I_{GND}	I_{LOAD}=0uA		0.7	2.0	mA
		I_{LOAD}=2A		4.8	8.7	mA
Shutdown Current	I_{GND_SD}	EN=0V, V_{IN}=5V		2		uA
Fixed Output Voltage Accuracy	V_{OUT}	I_{LOAD}=10mA, T_J=25℃	-1.5		+1.5	%
Adjustable Output Voltage Accuracy	V_{SENSE}	I_{LOAD}=10mA, T_J=25℃	1.182	1.2	1.218	V
Line Regulation	V_{LINE}	V_{IN}=(V_{OUT}+0.5V) to 6.5V	-0.1		0.1	%/V
Load Regulation	V_{LOAD}	I_{LOAD}=100uA to 2A		0.1	0.3	%/A
SENSE Input Bias Current	I_{SENSE}	100uA<I_{LOAD}<2A, V_{IN}=(V_{OUT}+ 0.5V) to 6.5V			1	uA
Dropout Voltage (note6)	$V_{DROPOUT}$	I_{LOAD}=500mA, V_{OUT}=3.3V		50	80	mV
		I_{LOAD}=1A, V_{OUT}=3.3V		100	160	
		I_{LOAD}=2A, V_{OUT}=3.3V		200	320	
Noise Spectral Density	OUT_{NOISE}	10Hz to100kHz, all fixed output voltages		6		uVrms
		100Hz to100kHz, all fixed output voltages		5		uVrms
Power Supply Rejection Ratio	PSRR	100kHz, V_{IN}=4V, V_{OUT}=3V, I_{LOAD}=1.5A, C_{SS}=0		60		dB
		100kHz, V_{IN}=3.5V, V_{OUT}=3V, I_{LOAD}=1.5A, C_{SS}=0		50		dB
		100kHz,V_{IN}=3.3V,V_{OUT}=3V, I_{LOAD}=1.5A,C_{SS}=0		40		dB
		1MHz, VIN=4.0V, V_{OUT}=3V, I_{LOAD}=1.5A, C_{SS}=0		30		dB
		1MHz, V_{IN}=3.5V, VOUT=3V, I_{LOAD}=1.5A, C_{SS}=0		30		dB
		1MHz, V_{IN}=3.3V, V_{OUT}=3V, I_{LOAD}=1.5A, C_{SS}=0		20		dB
Transient Load Response	t_{TR_REC}	Time for output voltage to settle within ±V_{SETTLE} from V_{DEV} for a 1mA to 1.5A load step, load step rise time=400ns		1.5		us
	V_{DEV}	Output voltage deviation due to 1mA to 1.5A load step		35		mV
	V_{SETTLE}	Output voltage deviation after transient load response time (t_{TR-REC}) has passed, V_{OUT}=5V, C_{OUT}=4.7μF		0.1		%
START-UP Time (note 7)	t_{START}	V_{OUT}=5V, C_{SS}=0nF		380		us

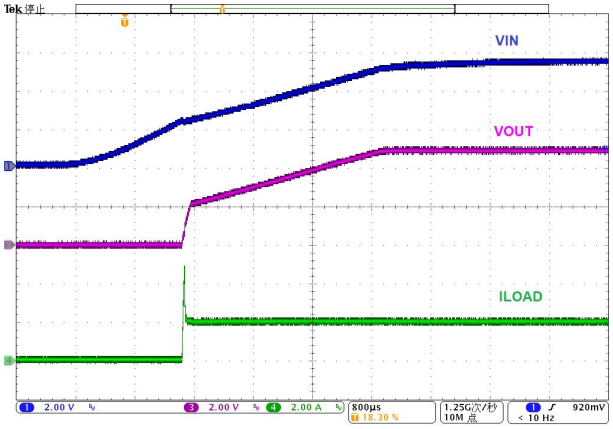
		V_{OUT}=5V, C_{SS}=1nF		1.0		ms
Soft Start Current	I_{SS}	V_{IN}=5V		1		uA
Current Limit Threshold (note 8)	I_{LIMIT}			3.3		A
VOUT Pull Down Resistance	R_{DIS}	EN=0V, V_{OUT}=1V		4		KΩ
Thermal Shutdown Threshold	TS_{SD}	T_J Rising		150		℃
Thermal Shutdown Hysteresis	TS_{SD_HYS}			15		℃
Input Voltage Rising	$UVLO_{RISE}$				2.28	V
Input Voltage Falling	$UVLO_{FALL}$		1.94			V
Hysteresis	$UVLO_{HYS}$			200		mV
EN Input Logic High	EN_{STBY_HIGH}		1.1			V
EN Input Logic Low	EN_{STBY_LOW}				0.4	V
EN Input Logic Hysteresis	EN_{STBY_HYS}			45		mV
EN Input Logic High	EN_{HIGH}		1.11	1.2	1.27	V
EN Input Logic Low	EN_{LOW}		1.01	1.1	1.16	V
EN Input Logic Hysteresis	EN_{HYS}			100		mV

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
Note 2. Devices are ESD sensitive. Handling precaution recommended.
Note 3. θJA is measured in the natural convection at TA=25°C on a high effective thermal conductivity test board (40mm x 40mm x 1.6mm double sided board with 2oz, copper ratio: approx. 50%) of JEDEC 51-7 thermal measurement standard.
Note 4. The device is not guaranteed to function outside its operating conditions.
Note 5. The output current at which the output voltage becomes 95% of VOUT after gradually increasing the output current.
Note 6. The dropout voltage is defined as VIN - VOUT, which is measured when VOUT is 98%*VOUT.
Note 7. Start-up time is defined as the time between the rising edge of EN to 90%*VOUT of its normal value.
Note 8. Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.3V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.3V, or 2.97V.

Typical Characteristics

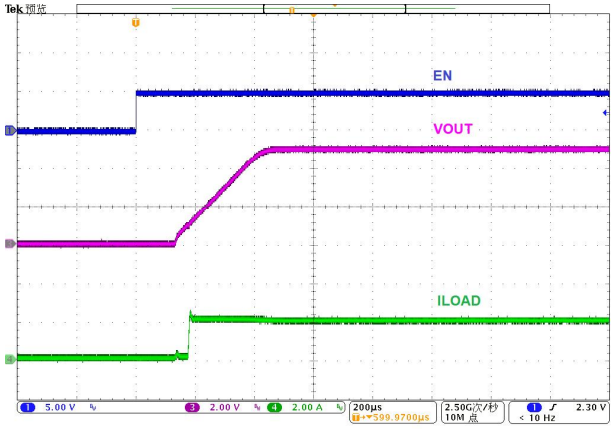
(T_A = 25°C, C_{IN}=4.7uF, C_{OUT}=4.7uF, unless otherwise specified)

Power On from V_{IN} With 2A LOAD



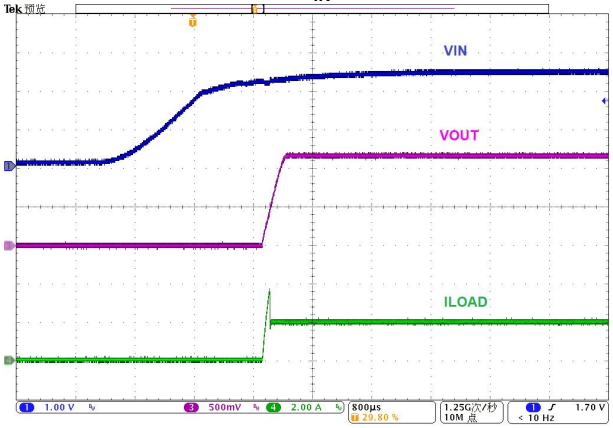
V_{IN}=5.5V, V_{OUT}=5.0V, ILOAD=2.0A

Power On from EN With 2A LOAD



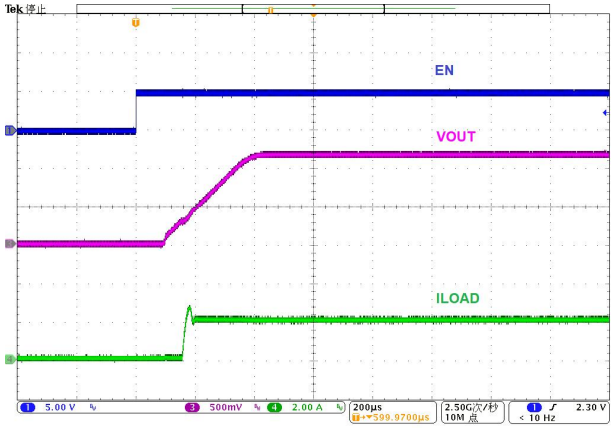
EN=5.0V, V_{IN}=5.5V, V_{OUT}=5.0V, ILOAD=2.0A

Power On from V_{IN} With 2A LOAD



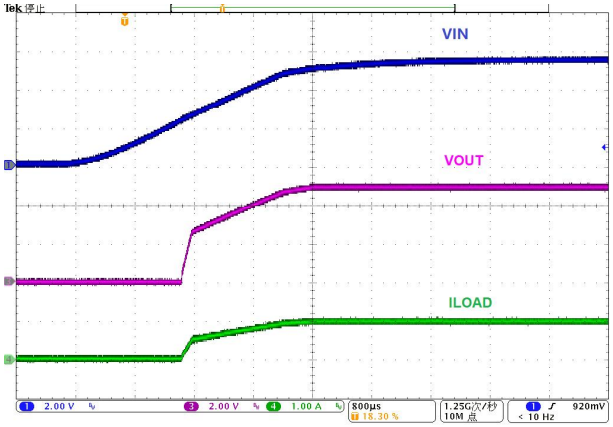
V_{IN}=2.5V, V_{OUT}=1.2V, ILOAD=2.0A

Power On from EN With 2A LOAD



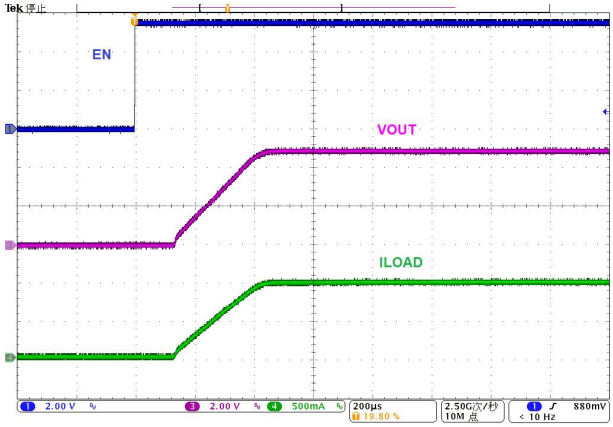
EN=5.0V, V_{IN}=2.5V, V_{OUT}1.2V, ILOAD=2.0A

Power On from V_{IN} With 5ohm LOAD



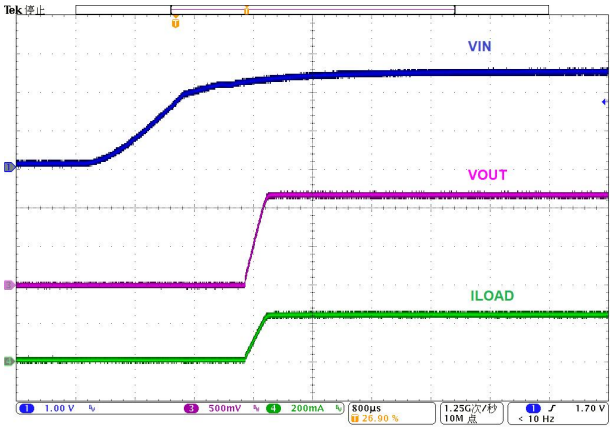
V_{IN}=5.5V, V_{OUT}=5.0V, RLOAD=5ohm

Power On from EN With 5ohm LOAD



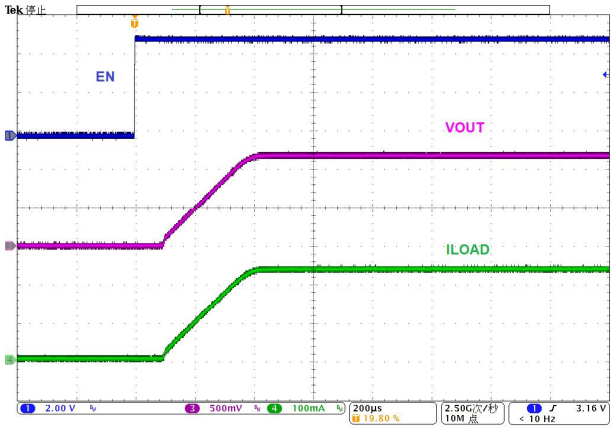
EN=5.0V,V_{IN}=5.5V, V_{OUT}=5.0V, RLOAD=5ohm

Power On from V_{IN} With 5ohm LOAD



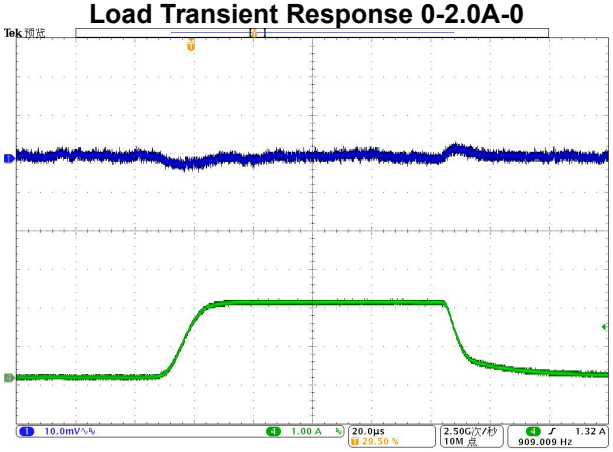
V_{IN}=2.5V, V_{OUT}=1.2V, RLOAD=5ohm

Power On from EN With 5ohm LOAD



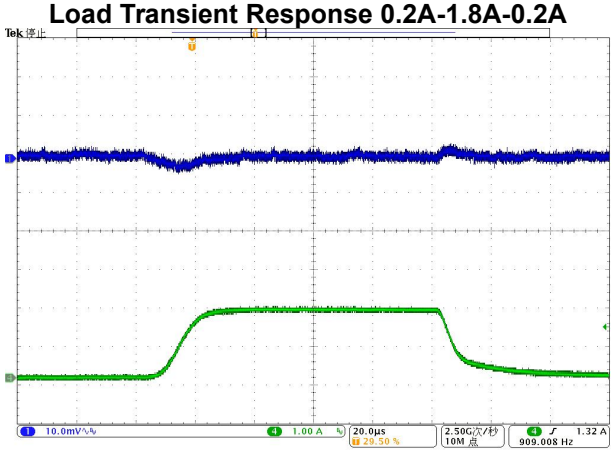
EN=5.5V, V_{IN}=2.5V, V_{OUT}=1.2V, RLOAD=5ohm

Load Transient Response 0-2.0A-0



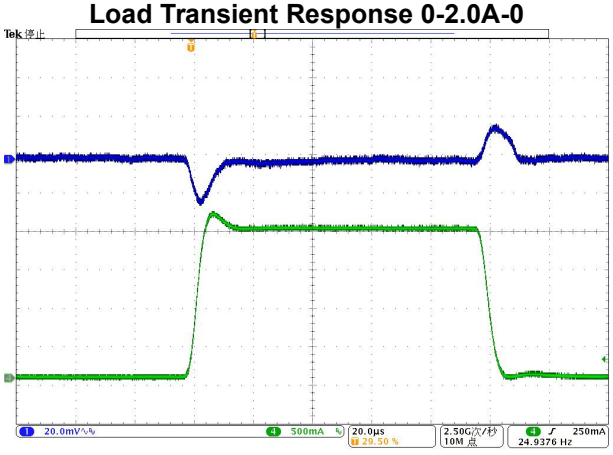
V_{IN}=2.5V, V_{OUT}=1.2V, ILOAD=0-2.0A-0

Load Transient Response 0.2A-1.8A-0.2A



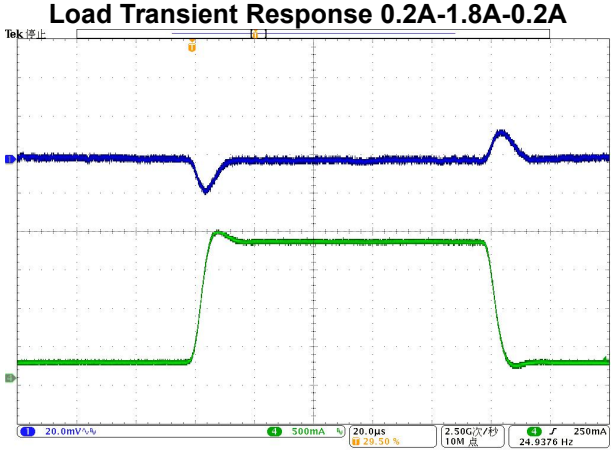
V_{IN}=2.5V, V_{OUT}1.2V, ILOAD=0.2A-1.8A-0.2A

Load Transient Response 0-2.0A-0



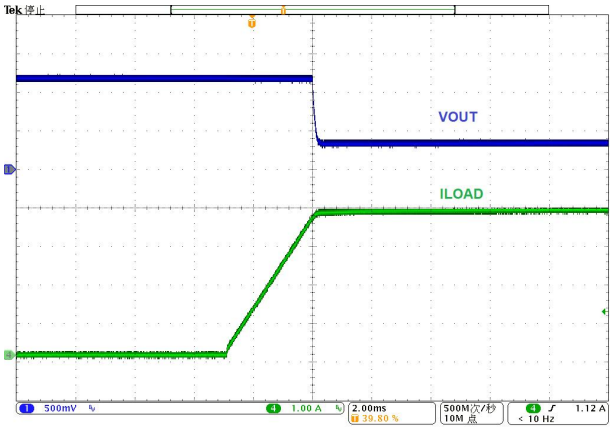
V_{IN}=5.5V, V_{OUT}=5.0V,ILOAD=0-2.0A-0

Load Transient Response 0.2A-1.8A-0.2A



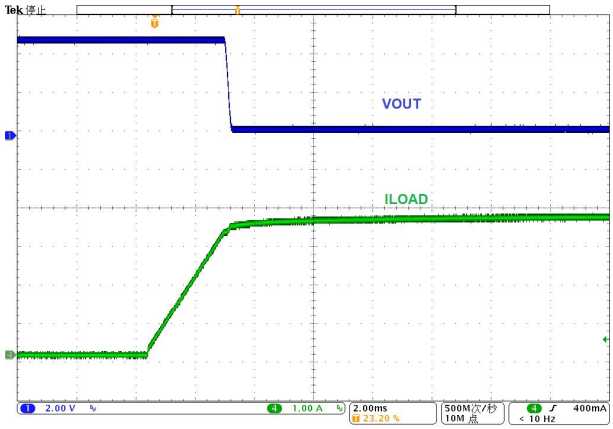
V_{IN}=5.5V, V_{OUT}=5.0V, ILOAD=0.2A-1.8A-0.2A

Over Current Limit



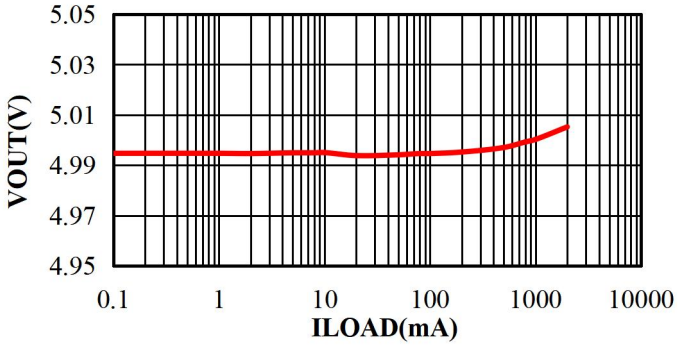
V_{IN}=2.5V, V_{OUT}=1.2V

Over Current Limit



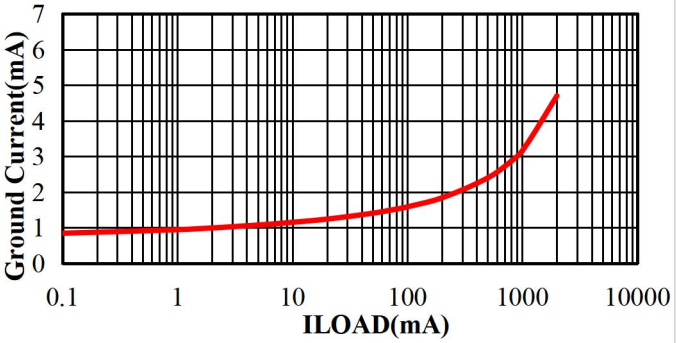
V_{IN}=5.5V, V_{OUT}=5.0V

Output Voltage vs. Load Current



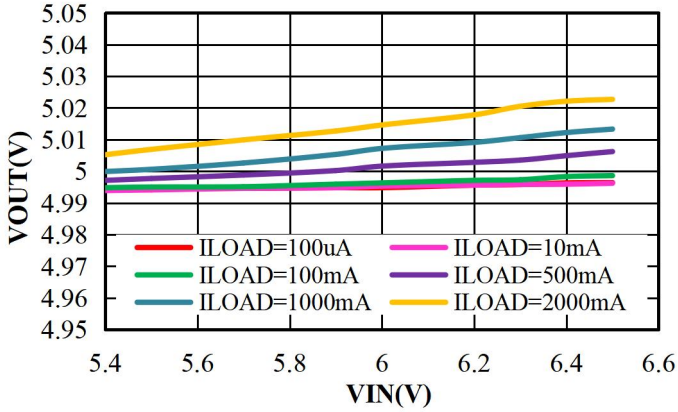
V_{IN}=5.5V, V_{OUT}=5.0V, ILOAD=0-2.0A

Ground Current vs. Load Current



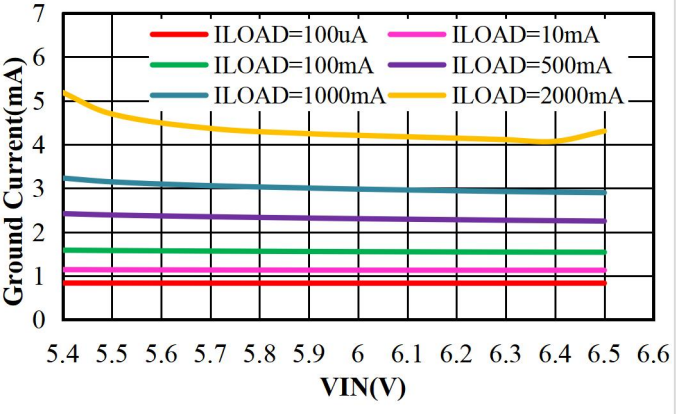
V_{IN}=5.5V, V_{OUT}=5.0V, ILOAD=0-2.0A

Output Voltage vs. Input Voltage



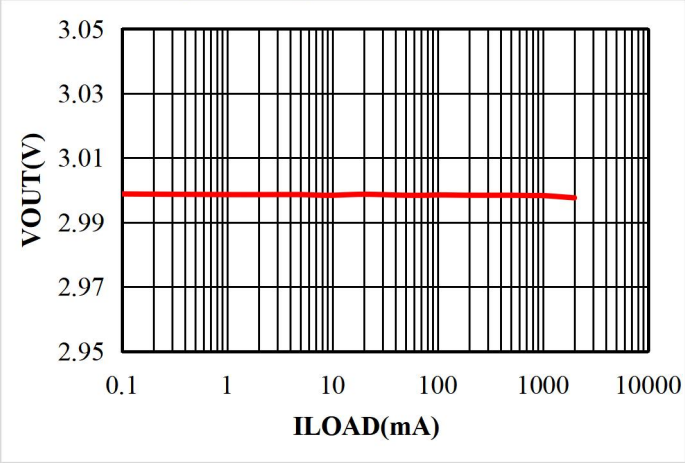
V_{IN}=5.4V-6.5V, V_{OUT}=5.0V

Ground Current vs. Input Voltage



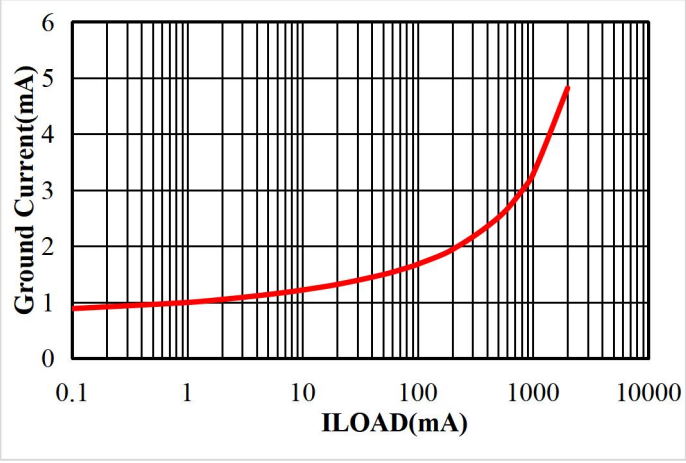
V_{IN}=5.4V-6.5V, V_{OUT}=5.0V

Output Voltage vs. Load Current



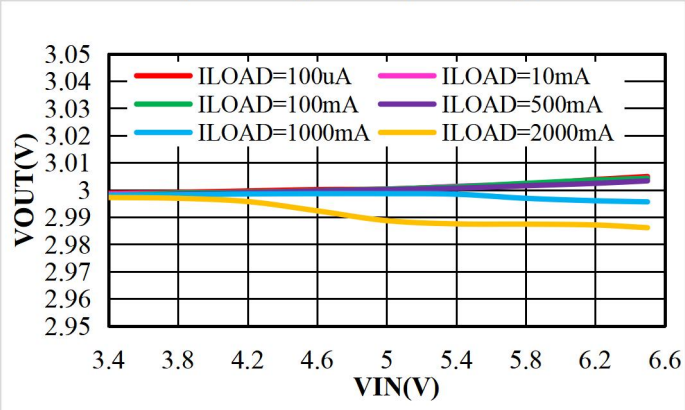
V_{IN}=3.5V, V_{OUT}=3.0V ILOAD=0-2.0A

Ground Current vs. Load Current



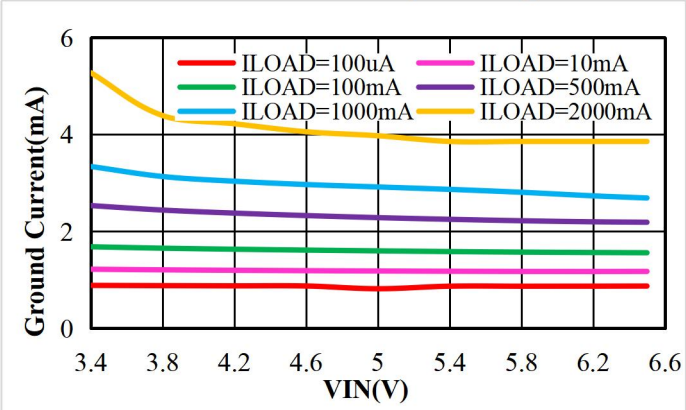
V_{IN}=3.5V, V_{OUT}=3.0V ILOAD=0-2.0A

Output Voltage vs. Input Voltage



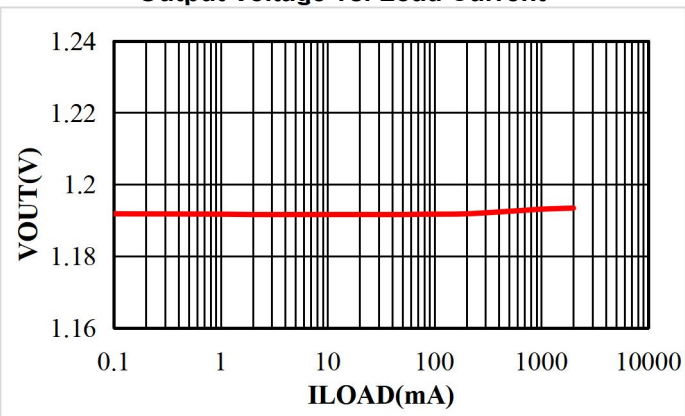
V_{IN}=3.4V-6.5, V_{OUT}=3.0V

Ground Current vs. Input Voltage



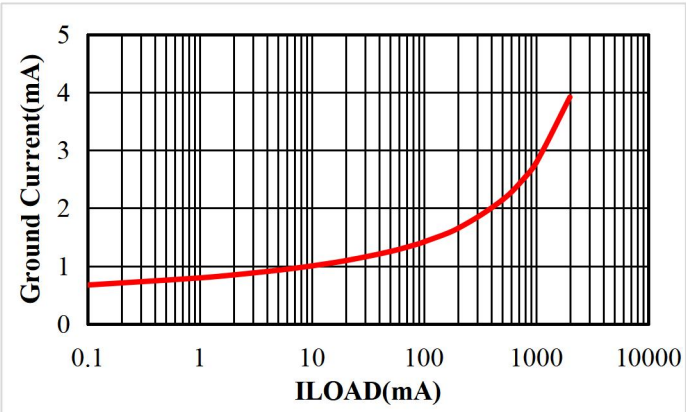
V_{IN}=3.4V-6.5, V_{OUT}=3.0V

Output Voltage vs. Load Current



V_{IN}=2.5V, V_{OUT}=1.2V ILOAD=0-2.0A

Ground Current vs. Load Current



V_{IN}=2.5V, V_{OUT}=1.2V ILOAD=0-2.0A

Application Information

Input Capacitor

A 4.7uF input capacitor or greater located as close as possible to the IC is necessary to ensure device stability. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. The X7R or X5R capacitor should be used for reliable performance over temperature range.

Place the capacitors physically as close as possible to the device with wide and direct PCB traces. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes.

Output Capacitor

The CL7172 is specifically designed to employ ceramic output capacitors as low as 4.7uF, ceramic X7R or X5R type due to its low capacitance variations over the specified temperature range.

The ceramic output capacitors connected as close as possible to the output and ground pins.

Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. Output current is internally limited to 3.3A typically.

OTP Protection

A Thermal shutdown protection circuit disables the CL7172 when the junction temperature of the pass transistor rises to 150℃(typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to 135℃ (typical).

The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Enable

The LDO uses the EN pin to enable its operation. If the EN pin voltage is < 0.4 V, the regulator will be turned off, reducing the supply current to less than 2uA. If the EN pin voltage is > 1.2 V, the regulator will be turned on. The EN pin has internal pull−down current source with value of 0.3uA (typical), which assures the device is turned off when the EN pin is unconnected.

Power Dissipation

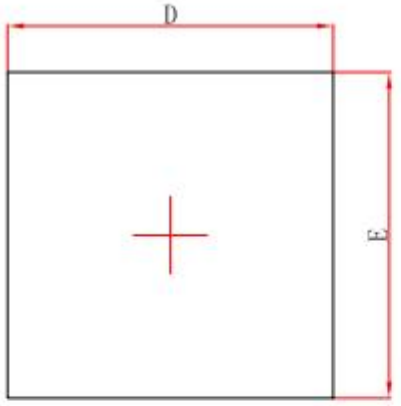
Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

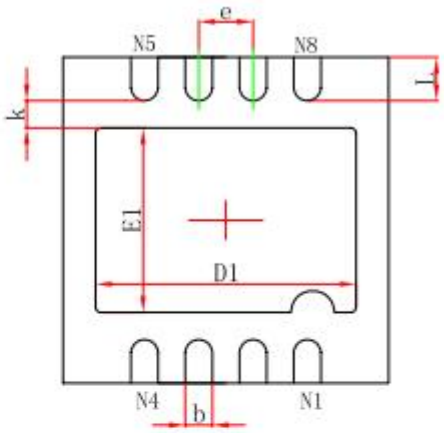
$$PD = (VIN - VOUT) \times IOUT$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails.To avoid thermally overloading the CL7172, refrain from exceeding the absolute maximum junction temperature rating of 155° C under continuous operating condition. Over-stressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

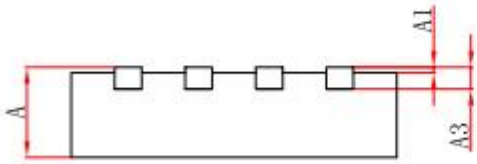
Package Dimensions: DFN3×3-8L



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

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